The Institute of Marine Engineers

One day seminar

PEBB

The future of power electronics?

London, Monday 6 July 1998

Chairman:

Cdr Chris Hodge **CEng, FIMarE**, *Cambridge Control Ltd*

Speakers include:

Terry Ericsen, *Office of Naval Research*

Dr Victor Temple, *Harris Semiconductor*

Dr Harshad Mehta, *Silicon Power Corporation*

Mischa Kyanin, *EUCLID Industry Group*

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13. ABSTRACT *(Maximum 200 words)*

Power Electronic Building Blocks (PEBBs) are power processors. A PEBB is not a specific semiconductor material, not a device, nor a circuit topology. It is the search for the most common denominator of all these things. It is not; "one size fits all." there will be several blocks that will fit together to perform the majority of every day power electronic jobs. Like a set of children's interlocking blocks, PEBBs will be a rational and simple set of blocks and procedures that most any designer or architect can use to build electrical systems.

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PEBB
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SEMINAR PROGRAMME

Chairman: Cdr C J Hodge
Business Manager, Power Systems, Cambridge Control Ltd, UK

0915 Registration and coffee

1000 **A study of Power Electronic Building Block (PEBB) form**
Speaker: Terry Ericsen
Program Officer, Electric Power, Office of Naval Research, USA

1100 Discussion

1120 **PEBB toolbox technologies – devices to systems**
Speaker: Dr Victor Temple
Director, Harris Power R&D, Harris Semiconductor, USA

1220 Lunch

1330 **HPEBB overview**
Speaker: Dr Harshad Mehta
President and CEO, Silicon Power Corporation (SPCo), USA

1430 Discussion

1500 Tea

1530 **The European industry perspective**
Speaker: Mischa Kyanin
Chairman, EUCLID Electrical Engineering Industry Group
Manager (Netherlands) Defence activities, IMTECH Marine & Industry/R&H Systems, The Netherlands

1600 **Panel discussion**
The implications to the European industry of the US PEBB initiative, from both a government and industrial viewpoint

1730 Informal reception

A Study of Power Electronic Building Block (PEBB) Form

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Abstract

There comes a time when small "evolutionary" changes are no longer adequate. Major changes must occur for progress to occur. Such a time is this in power electronics. Power electronic technologies, methods of manufacture and concepts must change radically for progress to occur.

The Office of Naval Research (ONR) is developing Power Electronic Building Blocks to achieve: increased power density, "user friendly" design ("plug and play" power modules), and multi-functionality. Digital controls, integrated with higher frequency and more robust power circuits, enable modular power systems with lower size, weight, and cost -- while increasing performance.

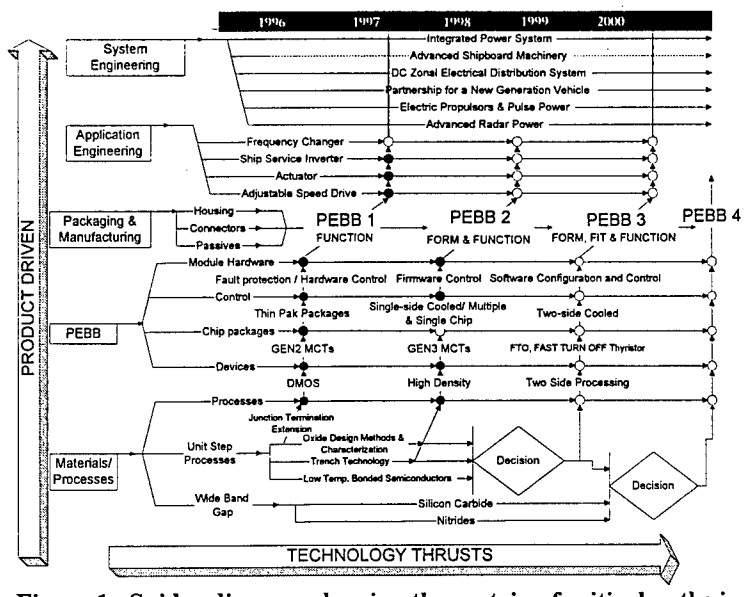


Figure 1. Spider diagram showing the matrix of critical paths in the PEBB program

Power Electronic Building Blocks (PEBBs) are power processors. A PEBB is not a specific semiconductor material, not a device, nor a circuit topology. It is the search for the most common denominator of all these things. It is not; "one size fits all." There will be several blocks that will fit together to perform the majority of everyday power electronic jobs. Like a set of children's interlocking blocks, PEBBs will be a rational and simple set of blocks and procedures that most any designer or architect can use to build electrical systems.

PEBB Program

Further details on the PEBB program are in references [1] and [2]. The summary herein updates the program and provides context for those unfamiliar with PEBB.

The Navy is challenged by the need for affordability. The total cost of Navy systems must be reduced. Beyond the cost of purchase, life-cycle costs (such as: manning, maintenance and fuel) must also be reduced. Performance must not be compromised; to the contrary, reliability and performance must be increased.

Using concurrent engineering in cooperation with academia and industry, the ONR program will develop PEBBs and associated technologies. Multipurpose, universal devices, will replace several specialized devices like circuit breakers, motor controllers, and power conditioners. Standardized manufacture will enable production of these devices in large quantities with reduced cost.

A "spider web" or "spider" diagram of the PEBB program, Figure 1, shows the integration of science and technology with engineering development leading to intermediate products and four targeted PEBB applications. Science and technology are proceeding along the horizontal axis, while products are drawn from the technical results

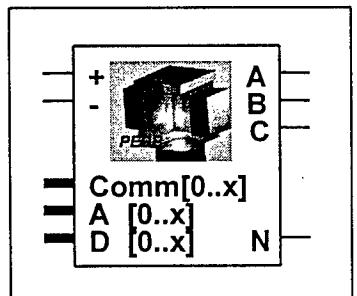


Figure 2. Power Electronic Building Block

in phased intervals.

PEBB-1, the first phase, demonstrated that multiple applications could be satisfied using the same set of hardware. Each application had its own set of software instructions. PEBB-1 proved that a single set of hardware could perform many functions, such as: motor control, actuator control and power supply.

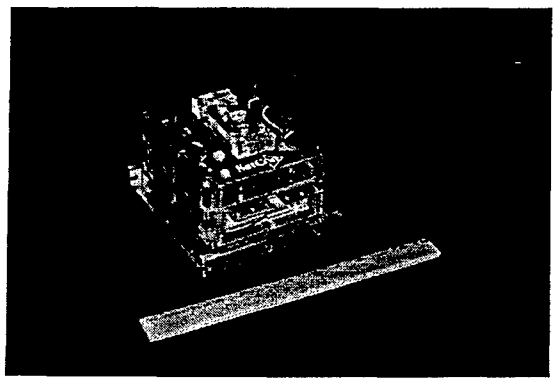


Figure 3. 50kW, 3-phase inverter by SATCON (~400 kW/ft3 or ~14.1MW/m^3)

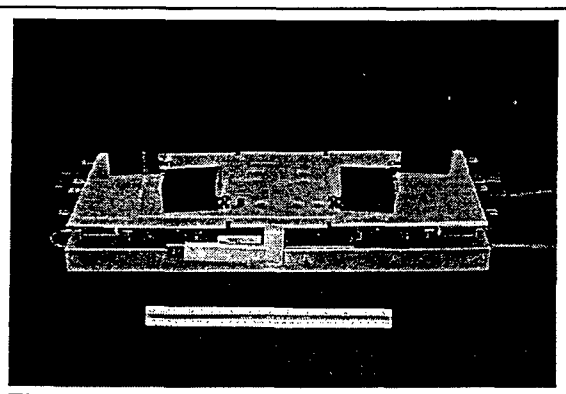


Figure 4. 250kW, single phase leg of a 3-phase multi-level inverter by VPI&SU (200-250 kW/ft^3 or 7.1 – 8.8 MW/m3)

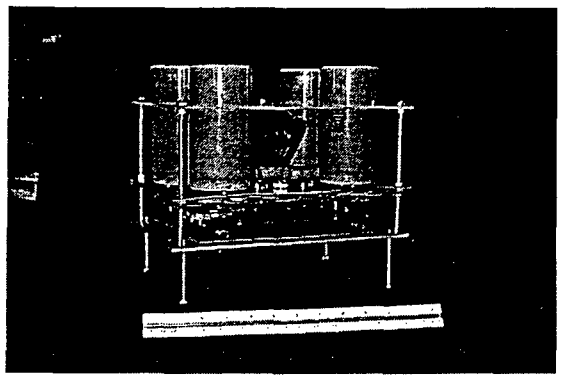


Figure 5. 250kW, single phase leg of a 3-phase inverter by DNSWC/Harris (60 - 80 kW/ft3 or 2.1 – 2.8 MW/m^3)

The Navy program defines the first PEBB device as a five power port device – 2 DC and 3 AC/DC ports as shown in Figure 2, also see reference [3]. This device corresponds roughly to a 3-phase bridge. The three AC/DC ports are programmable waveform ports. Within the bandwidth of the device, the waveforms at these ports are completely controllable by software programming. In addition to the power ports, there is a communication bus (Comm [0...x]), an analog bus (A [0...x]) and a digital bus (D [0...x]). Making only external connection changes, PEBB-1 demonstrated the following applications: a) DC to AC inverter, b) AC to DC converter, c) DC to AC motor controller, d) AC to DC boost converter and e) DC to DC boost converter, see [3].

PEBB-2, the subject of this paper, focuses on developing and defining PEBB form. PEBB form is defined primarily by packaging considerations such as thermal, EMI, interconnections, interfaces, communications, sensors, control, manufacturing economics, reliability, passive devices, etc. PEBB-2 will demonstrate higher-power and faster-switching devices. PEBB-2 will also demonstrate tighter power and micro electronic integration.

PEBB-3 will demonstrate a fully optimized PEBB prototype in form, fit, and function. The critical technological improvements manifested in PEBB-3 are the use of two-sided cooling, ultra-fast turn-off thyristors, distributed/integrated control architecture with software configuration and control. A system designer, with minimal power background, will be able to construct an electric power machine by using these standard-building blocks, quickly, simply, reliably.

General PEBB Form

As a beginning to the study of form, three PEBB-2 concept demonstrators were built – figures 3,4,5. All three designs used different assumptions and different technologies from the PEBB program. However, all three exceed the PEBB program power density goal of 50kW/ft^3 (1.8 MW/m^3). The Satcon version shown in Figure 3 illustrates that for power ratings of 50kW or less and lower voltages (~350V) a complete three phase inverter in a module is reasonable. On the other hand, 250kW 3phase inverters will most likely be in multiple modules, as

evidenced by Virginia Tech's[4] and CDNSWC/ Harris' Work.

PEBB Design Elements. Filters comprise 2/3 the size and ¾ the weight of Navy equipment. If the size and weight of the filter can be significantly reduced, then the equipment can be reduced accordingly. Increasing switching or circuit frequency and replacing passive filtering with active filtering was the most reasonable approach.

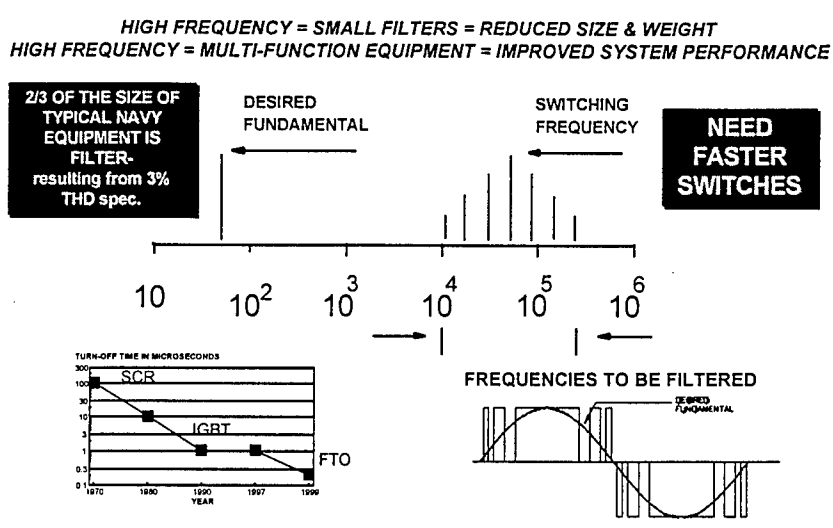


Figure 6

Actualization of high frequency switching requires faster switches. Faster switching increases switching losses. Increased switching losses also favor circuits that minimize or eliminate losses -- zero current or voltage switching. Power circuit packages with ultra-low inductance and controlled parasitic elements are necessary. All digital control circuits that use microprocessors and EPLD (Erasable Programmable Logic Devices or gate arrays) are needed to accommodate the endless variety of control algorithms.

In figure 6, the general idea of increased frequency and reduced filter size is illustrated. The higher the frequency of the filter, the lower the value of inductance and capacitance needed. In the Figure 6, the PWM (Pulse Width Modulation) scheme shown is variable frequency. The pulse widths change and so does the starting point for every switching cycle. The approach minimizes the number of switching events during a cycle of the desired fundamental produced. Thus, switching losses are minimized. However, varying switching frequency produces varying harmonics in the spectrum. The spectrum shown, with a single switching frequency and a clean band between it and the desired fundamental, cannot be obtained using a variable frequency PWM.

Fixed frequency PWM (Figure 7) must be used to get the spectrum shown. In this case, the total switching interval or cycle is always the same length of time. The switch duty cycle changes every cycle to produce the desired fundamental. Switching losses are greater than the previous case, because switching occurs every switching interval -- even if the output is not different from the ideal reference.

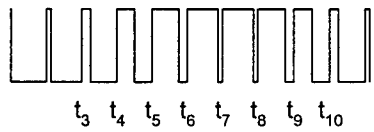


Figure 7

In the first case, the switching frequency is varied, losses are minimized, and the filter is larger -- because of the additional low frequency harmonics. In the second case, the switching frequency is constant, the filter is smaller and the switching losses are greater. So, for a given input and output filter configuration, harmonic distortion and switching losses can be traded off.

Basic Power Blocks. Looking a bit more closely into designs of figures 3,4,5, one can see the relationship shown in figure 8. These are the four major sections of a PEBB. A Navy PEBB will have these same blocks independent of weather the power

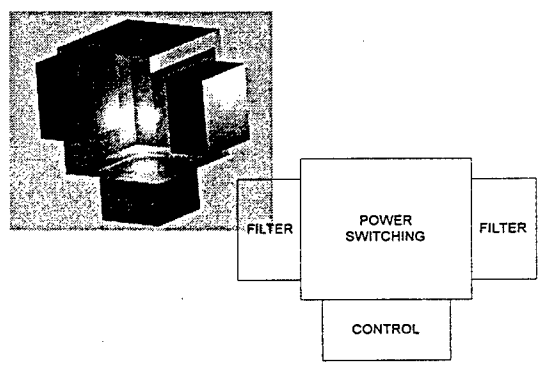


Figure 8. Four major PEBB partitions

switching is a simple switch, a switching phase leg, or a full three-phase bridge. Furthermore, this would also be true if the PEBB were designed on a single VSLI microchip or if each of the parts was housed in separate buildings for utility applications. In other military and industrial applications, the definition of what constitutes a filter, or if there are input or output filters at all, are the defining questions.

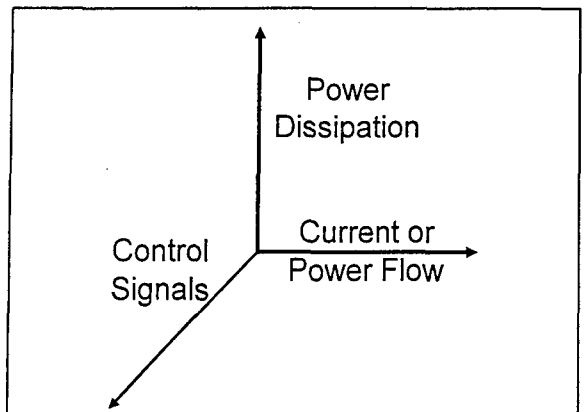


Figure 9. Orthogonal Axes of Design

The search for the most common technical denominators of power electronics begins with this kind of "fractal" definition. The building block metaphor is rooted in our universal use of superposition in power electronic design. A universal power electronic definition, unlike an official language, must have the support of physics first and consensus second.

As a beginning, Figure 9 pictures three orthogonal axes. All power electronic designs share these constraints. Signal and power lines need to be 90^0 from each other. This affords the minimum electromagnetic coupling and thus minimum interference of power switching on the control and sense signals. The power dissipation path should have a large surface area for minimum thermal resistance or maximum heat conduction. One does not wish to conduct heat through the control electronics. They are far less tolerant of heat. In the same way, heat conduction through filer capacitors and inductors, which are along the power-flow path, is also not reasonable. A natural direction for heat flux is 90^0 from both signal flow and power flow. In one ideal, power modules would be flat with signals paths aligned to two edges and with power at the other two perpendicular edges, and two large flat surfaces for single or double side cooling.

Finally, these blocks become the major partitions in which design expertise can be concentrated. Digital control experts could work independently with standard power and filter block emulators. Power circuit designers could use off-the-shelf controllers to develop new topologies. Standard interfaces would be specified between these blocks, and open architecture can occur by allowing ones control block design to plug in someone else's power block design.

The University of Wisconsin-Madison team, headed by Tom Lipo, extended this definition with the application-level PEBB or APEBB[5]. The APEBB, shown in figure 10, adds more detail to the same four major partitions. The signal paths are perpendicular to the power paths. The heat path is perpendicular to the power path and opposite to the signal path. This conforms to the desire not to conduct heat through the control electronics and is another variation.

In figure 10, interface requirements and signals are beginning to be defined. Electrical isolation is placed between the control and power blocks -- rather than between the control block and the rest of the world. Other needed blocks such as sensors, onboard power, and gate drives are placed in the power block. Interface control and feedback signals have a first order definition.

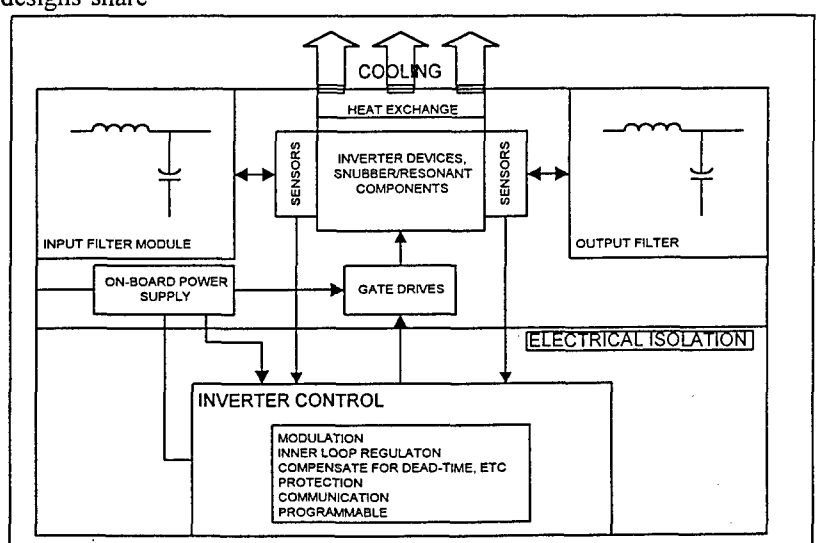


Figure 10. APEBB, spatial partitions after Deepac Divan

PEBBs are combined to perform system functions, as shown in Figure 11. Multiple PEBB

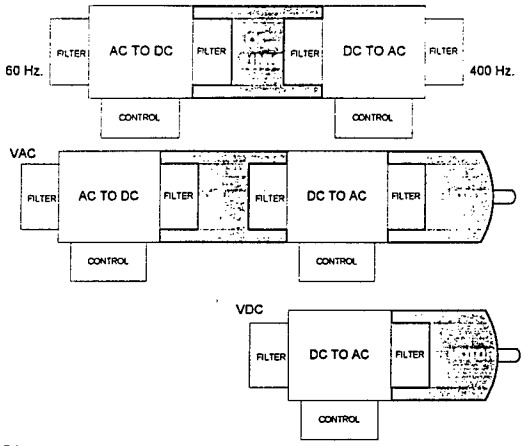


Figure 11. Top, 60 to 400 Hz. Frequency Conversion using two PEBB inverters (made of switching, filter and control blocks) and a DC Link. Middle, AC to AC motor controller using two PEBBs. Bottom, motor controller feed from a DC source.

modules would perform system functions, such as: voltage scaling, energy storage and impedance matching. This is the kind of top-level description needed for higher level design by architects and system engineers.

For example, the simplest frequency changer is made of a converter, an inverter and a DC Link. In figure 11, a frequency changer is made of 2 PEBBs and a DC Link building block. One PEBB is programmed as a boost converter (rectifier) and the other an inverter. Each PEBB is comprised of power switching, filter and control building blocks.

Other examples of PEBB form. Additionally, the Northrup-Grumman team headed by William Patalon confirmed the functional definition of a PEBB[6]. A partitioning of blocks or elements is proposed as shown in figure 12. This agrees very closely with the general PEBB form proposed herein.

Yet, another example is proposed by ABB as shown in figure 13. This time Pieder Jorg of ABB Corporate Research proposes a rack for the integration of power converters. Again, this version has converter blocks, filter blocks, energy storage blocks. This plug in version has the same five terminal definition, two DC and three AC ports. The modules or blocks are plugged into back-plane wiring. Water-cooling is across the bottom-plane. Figure 14 shows a converter module, which is plugged into the rack. A liquid cooled heat sink is mounted along the side of the converter module.

Open architecture is enabled in the same way as cards in an electronic rack system. The backplane adds impedance to the system, as compared to laminated buses. However, the circuit switching frequency is about 3kHz. The rack approach is reasonable in this frequency range and ABB uses input filtering to compensate for added bus impedance. In effect, this supports the use of a filter block at the input to the converter and is consistent with, in large part, with the partitions proposed in figure 9.

All of these approaches fit within the form proposed and confirm the general commonality of converters and inverters. In addition to physical partitions, time (response and control loop periods) must also be defined. Furthermore, they must be complimentary to the physical partitions for a truly common basis for power electronics design to emerge.

Temporal partitions[5]. There are temporal partitions for an advanced system of many PEBBs. Each system layer would have clearly defined control boundaries, as shown in Figure 15. Each control boundary would have a time interval associated with it. Hierarchical control functions combined with temporal partitions allow independent and parallel development of system elements. This further enhances "open architecture" in the final system.

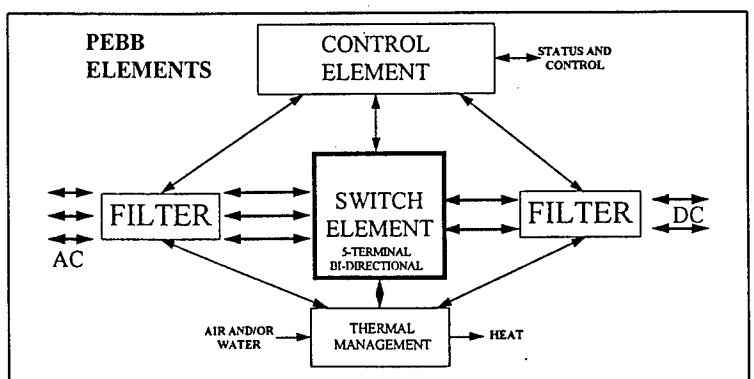


Figure 12. Northrup-Grummam PEBB elements

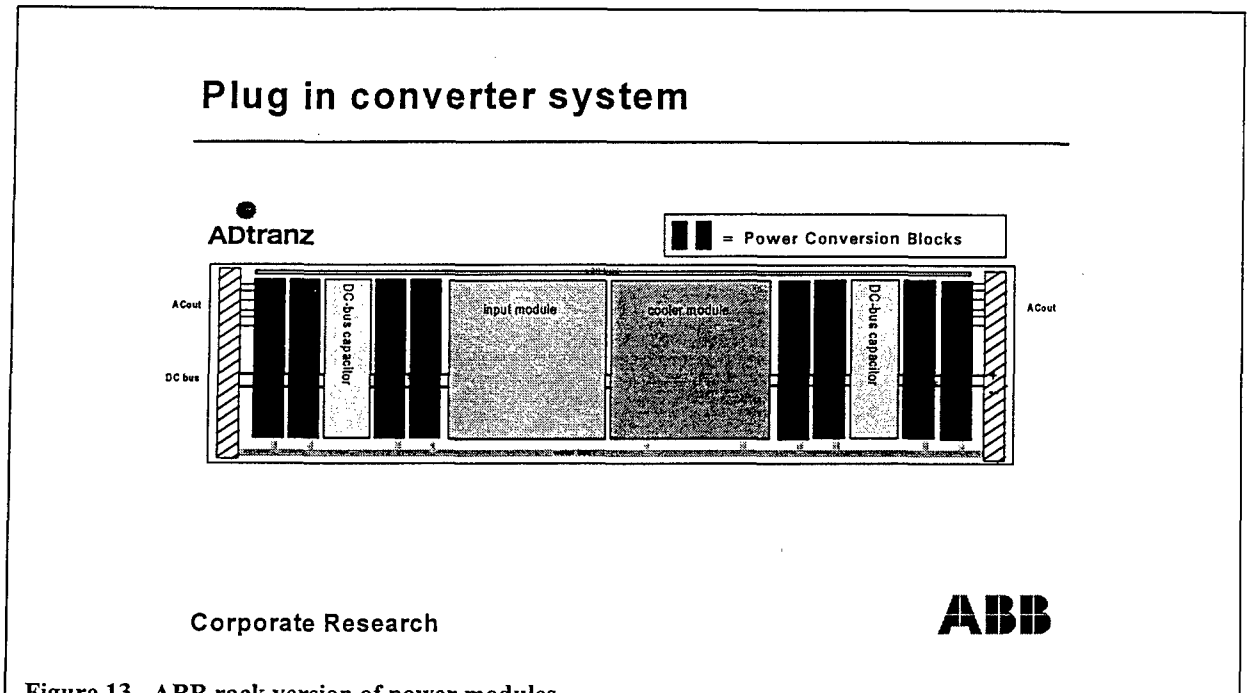


Figure 13. ABB rack version of power modules

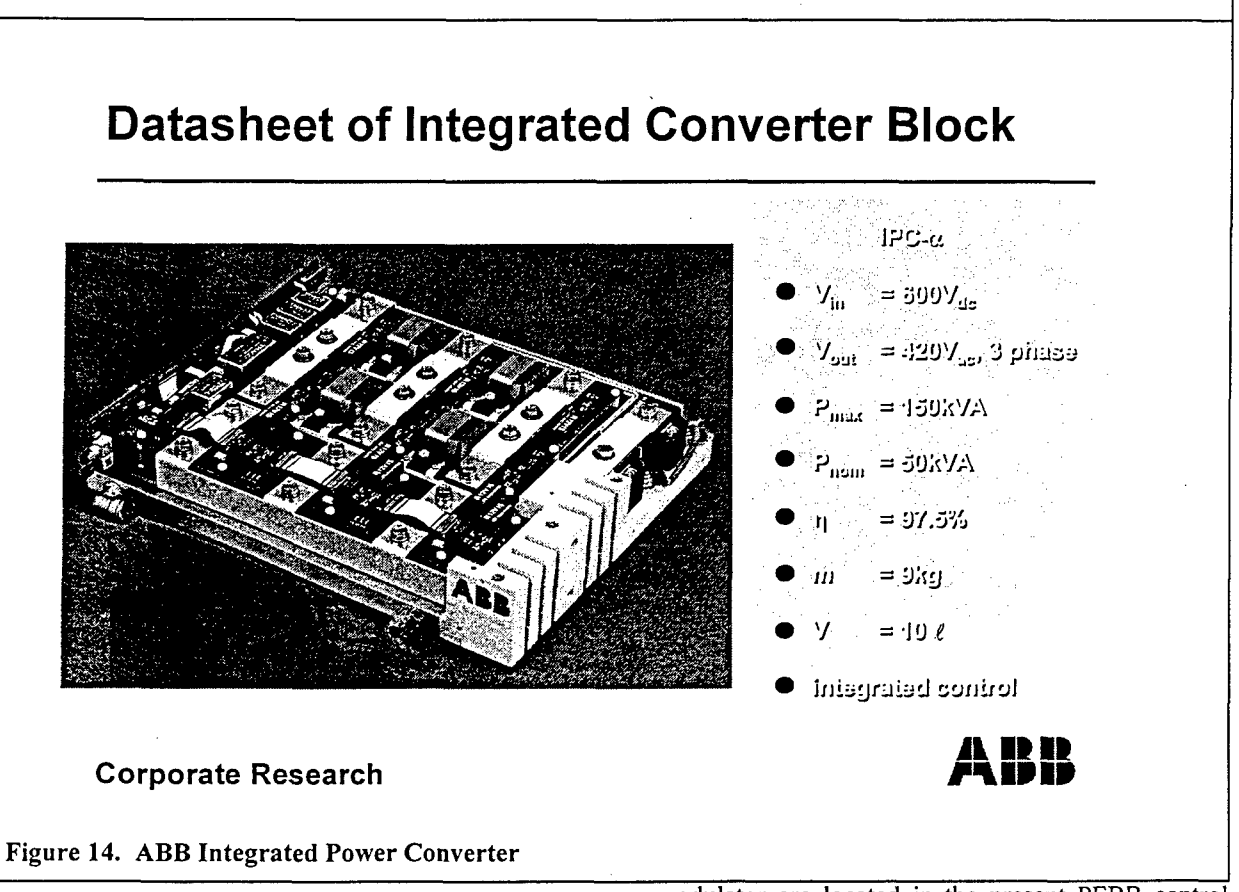


Figure 14. ABB Integrated Power Converter

The PEBB of figure 9 corresponds to the application invariant section of figure 15. Within the application invariant section, the inner loop and modulator are located in the present PEBB control block. The power module and the gate drive correspond to the power switch block. The filter mod. and switchgear correspond to the filter blocks

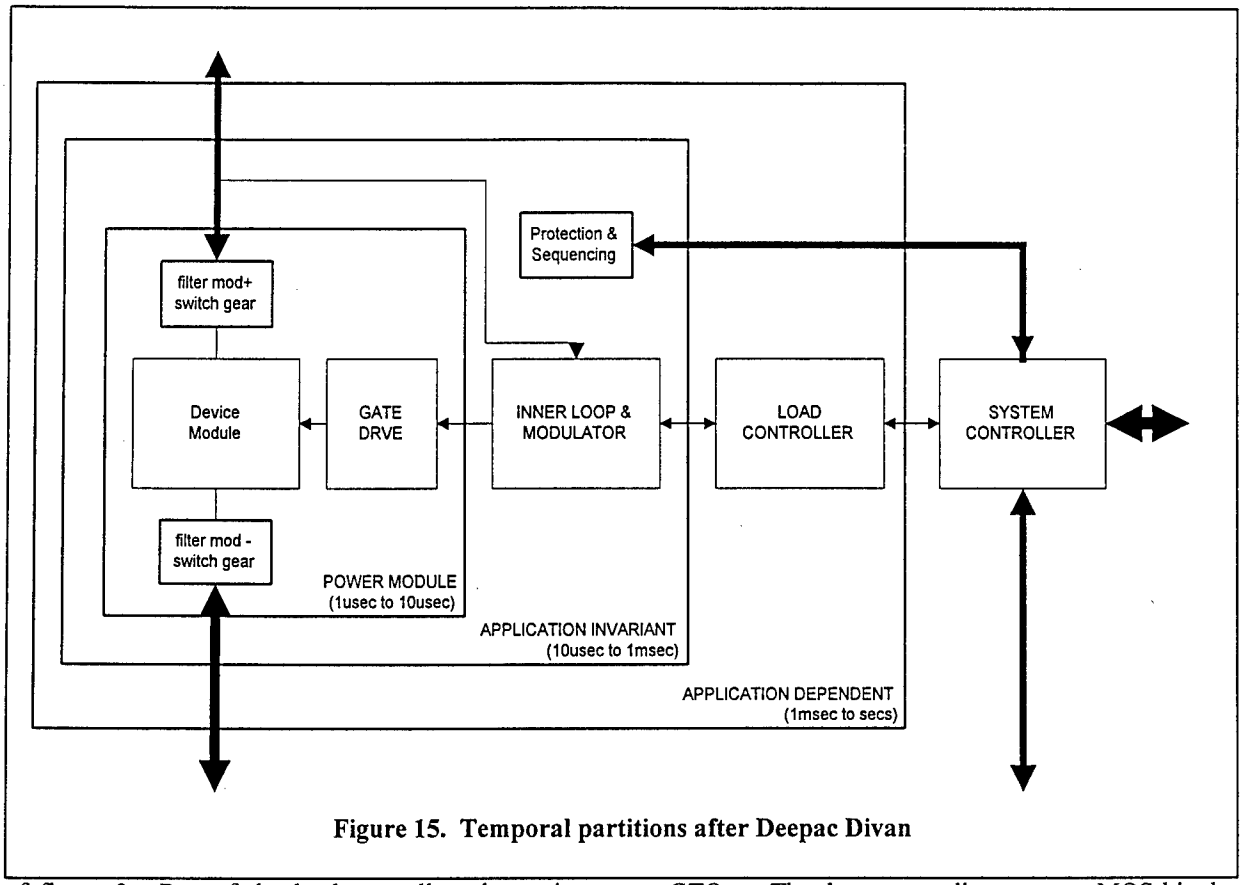


Figure 15. Temporal partitions after Deepac Divan

of figure 9. Part of the load controller, shown in figure 15, is in the control block. The system controller has not been defined and will need to be developed in the PEBB-3 phase. Furthermore, control functions as well "intelligence" will be distributed throughout the PEBB – creating intelligence partitioning as function of time and physical location.

Building Block Details

Before continuing globally, details of the parts must examined to strengthen the ideas proposed. Up to this time, there is no distinction of high or low power. The arguments have also been independent of the number phases, the type of circuit topology, or switching device.

Switching Block. The semiconductor chips dominate the form of the switching block. They are thin and flat, produce most of the heat, and control the electric power. The maximum junction temperature of these chips sets the primary ratings of the block, as well as the rest the PEBB.

Low power switches are mostly MOSFETs and MOS-bipolar devices -- IGBTs or MCTs. High power switches mostly bipolar devices -- SCR or GTOs. The low to medium power MOS-bipolar switching chip is not one device. It can be as many as two million devices in parallel in one chip. Each device is matched to the millions of other devices, because of the integrated circuit technology used to produce them. The millions of matched devices on each chip force current conduction to be uniform and the heat generated to be evenly distributed across the chip. These chips or dies are rectangular and the size is limited by manufacturing economic factors such as yield.

As the voltage and current increases, the semiconductor switch becomes again a single device per chip. This is the older power semiconductor technology that the MOS IC process has not yet been able to displace. The chip is now 55mm or greater in diameter and is really a wafer. High-power devices have ratings limited by hot spotting phenomena. The chip is circular instead of rectangular. The circular form follows the form of the wafer and is more high voltage capable. Controlling the electric field at the corners of the rectangular chip is a difficult edge termination design problem.

The thin, flat, forms of both of these chip technologies minimize thermal and electrical resistance. The maximum cross section and the least

conduction length is produced for a given switch voltage and manufacturing process. Lateral thermal and electrical conduction is restricted by very low cross sectional area and increased conduction length in lateral directions. Thus, electrode potential should be uniform across the entire conduction cross-section.

However, uniformity of the electrode potential is restricted by mechanical properties. The thermal coefficient of expansion of the metal electrodes and the silicon chip do not match. As the thickness of the metal increases, thermal cycling stresses between the material increases and failure occurs. Because of this, copper or aluminum electrodes are limited by the following alternatives: 1) the thickness must be limited to less than a few 100 micro-meters, 2) contact area must be limited or 3) no stiff bonding can be used.

The first issue is again the problem of non-uniform lateral conduction in the metal electrode when it is too thin and mechanical stress when it is too thick. In the second case, using wire bonding can make mechanically reliable contacts. However, current crowding in the semiconductor chip, this time, causes hot spots. The length of the wire reduces thermal and electrical conduction and increases inductance.

Pressing metal contacts against the front and back flat surfaces of the chip or wafer (used in high power devices) can also make reliable contacts. Thermal and electrical conduction is decreased by the "dry" interface between the metal contacts and the semiconductor wafer. However, in large (55mm) devices uniform contact potential is essential, even if thermal and electrical conduction is reduced slightly. Since the interface is not bonded, the surface can slide past one another, allowing expansion differences. A scrubbing between the surfaces occurs over a very long time, but the life of the device is decades.

"Thin-Pak" lids[7]. In the PEBB program, HTP packages were developed[6]. A ceramic lid is made the size of chip. Like a circuit board, holes are drilled to create paths for current conduction. Both sides of the ceramic are plated with metal and patterned for electrical connection. The holes are plated to electrically connect both sides. Areas are provided for control and power connections. The lid is then soldered to the chip. The resultant assembly pacifies the semiconductor junctions. The device can now be tested at full power, before continuing to next stage of packaging.

The ceramic thin-pak lid has a closely matching coefficient of thermal expansion to silicon. The lid also allows cooling on topside of the chip. Furthermore, the ceramic lid and the hole pattern create a distributed impedance to help spread the current and keep electrical resistance low. More work is needed to characterize and develop design methods for this technology. The lid adds cost compared to wire bonded packages; but the lid allows greater utilization of the chip and a better mechanical, thermal, and electrical tradeoff.

Switches. As stated earlier, a switch can be several millions of devices in parallel on one chip or it can be a single device on a large wafer. There are several chip sizes used in the program as seen in table 1.

These six sizes cover virtually the whole range of power electronic machines now made. Building up from this simple base, a set of blocks can be made that enable an enormous product range from a minimum of manufacturing variation, and, hopefully, cost.

Table 1

	Dimension	Size
Rectangular (millimeter x millimeter) low to medium Power	3.38 x 4.17	3
	6.6 x 10.2	6
	10.2 x 15.2	8
Circular (diameter in millimeters) high power	55	55
	77	77
	125	125

Assuming generic electrodes and packaging for all device types, a size 3, 5 or 8 chip could be a MOSFET, IGBT or MCT device -- depending only on the process selected. Standard chip sizing, electrode patterns and packages allow all other assembly steps to be unchanged. In the same way, a high power wafer could be a SCR or GTO. With MOSFET chips, the GTO wafer can be configured as an IGCT, MTO or ETO. The selection of the chip or wafer size (3,6,8,55,77,125) and the package sets the basis for power dissipation. Selection of the device type, sets the basis for performance and the characteristics possible -- within the chip or wafer size selected.

For example, size 3, 6 and 8 chips correspond to roughly 125, 600, 1400 Watt maximum dissipation. This assumes that they are silicon chips soldered to a base plate, which can be held to 90C, while the junction temperature is no more than 150C. One selects an IGBT, MCT or other device based on circuit requirements. The conduction, switching, and blocking losses set the maximum heat dissipation needed and thus the chip size selected.

The real design process is much more involved. However, a flexible semiconductor processing capability, combined with computer aided device and chip selection, could enable a design process as simple as this. The challenge in phase 3 of the PEBB program will be to do it.

Packaging. Continuing to build, the next step is mounting and packaging chips. The chip size is determined by manufacturing cost factors. Likewise, the switch assemblies and packages must be established based on manufacturing cost considerations. For example, there is a minimum 10% penalty for paralleling chips and a corresponding cost penalty for substrate size and mounting. A single chip has lower packaging costs but the cost of the chip is greater. Using a single chip or multiple chips in parallel is a tradeoff between cost of the larger chip and cost of paralleling smaller chips.

In low to medium power case, there are only three chip footprints. Some diode sizes are also needed. However, these relatively few pieces can form an endless array of power blocks. Chips mounted on a common substrate could be in parallel or connected into a circuit. The chips could be IGBT, MOSFETs, or MCTs -- based on the computer selection scheme above. Hard or soft switching types of circuits are formed; again using computer aided selection and interconnection of the chips.

With "Thin-pak" lids on the chips, an etched metal frame soldered to the array lidded chip forms the top circuit. The bottom circuit is formed from the metal layer bonded to the substrate. The process is very amenable to automation.

The PEBB-2 concept demonstrators showed that a whole 3-phase inverter (50kW or lower) could be an integrated into a module. At 250kW and above, only a single phase could be integrated into a module and three of these could be connected to make a three-phase inverter. Although auxillary cicuits could be integrated in the same single phase module as the main phase switches, it not likely to be economically efficient to do so unless usage of soft-switching topologies increases dramatically. At this level, the main switch is likely to be in one module; and any auxiliary switch used for soft switching would be in a separate module.

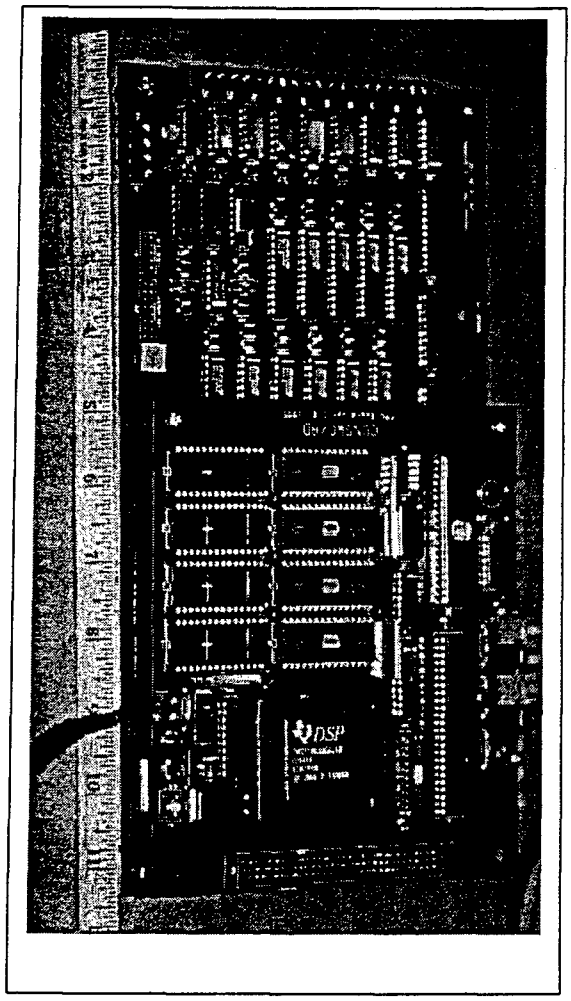
As the power increases, the larger device wafers are used. Again there are only three sizes. They are packaged as one device per package and circuits are formed by external device connections. This technology will continue to be labor intensive into the near future. However, there will be modules defined in same manner as the lower power counter parts. The generalized partitions and design concepts transcend the power boundaries and will increase manufacturing efficiencies at the very highest power.

Heat removal from the device package is an equipment or system design factor. For a given power package, the ultimate power handling capability depends on: liquid vs. air-cooling, single-side vs. double-side cooling, and other methods such as phase change cooling. These methods are a part of a thermal circuit that extends to the walls of the building or hull of the ship and beyond. These variables must be considered primarily in the design beyond PEBB. Thus, PEBB must provide the most reasonable thermal interface to larger design problem.

Filter Block. The classic input and output filters are low pass or integrating. Figure 10 shows a classic simple LC filter. More sophisticated filters, with many more poles, can be designed. However, with active filtering built into the inverter control algorithms, sophisticated filters will only be needed in custom applications. The problem is that the range of filter-cutoff frequencies and possible inductor and capacitor values are vast. Work will continue to define a set of capacitors and inductors to be formed into standard filter blocks.

Work is needed to reduce the size of storage and filter capacitors. DC link capacitors dominate the size of the inverters.

Digital Control Circuits. In the past, different inverter designs would require completely different control circuits. Today, the majority of inverter designs can be implemented using the same control circuit.



Digital control has really opened up the standard module possibilities. All digital control circuits use microprocessors and EPLD (Erasable Programmable Logic Devices or gate arrays). In fact, control circuits based on these technologies can accommodate just about any control algorithm or scheme with software changes only. These new controllers also allow dynamic changes in control during machine operation. Increased control and switching bandwidth allow power electronic machines to be electronically tuned or configured.

The PEBB-1 control circuit shown in Figure 16 uses two microprocessors and is laid out on two printed-circuit boards. The motherboard is about 6"x6". The daughter board is 6"x12". The control circuit will be substantially decreased in size, weight, and cost by using surface mount technology. In order to reach the final project goals, aggressive application of VLSI technology will be needed --PEBB-3.

Summarizing PEBB Details

Both high and low power devices are flat and thin. Gate or base control comes in from the side. Power is conducted through the device with the control surface (MOSFETS or inter-digitized base or gate structures) perpendicular to the power flow. All power devices have collateral power and heat flow at the large flat chip or wafer surfaces. At the external package terminals, power is conducted laterally by a laminated bus or cable to other circuit components. Heat continues on to some method of heat exchange. This is consistent with the orthogonal relationship proposed and is applicable to the very low and to the very high power devices. Furthermore, the electrical, thermal and mechanical requirements, which are at odds with each other, define the form of the power switching module and the final form of the whole PEBB.

A "do everything" power module is not realistic. However, a multi-functional set of building blocks that will fit together to satisfy 80% of the power electronic jobs, is. Like a set of children's interlocking blocks, PEBBs will be a rational and simple set of blocks and procedures that most any designer or architect can use to build electrical systems. Just one set of building blocks capable of the majority of the day-to-day jobs will enable a new, higher volume market to emerge.

The electrical, mechanical, and thermal form of a system of Power Electronic Building Blocks has been defined in a consistent, systematic, manner. Figure 17 identifies all the parts needed for standard PEBBs. A computer aided design and selection system is under development and will be used to simplify the power electronic design. This Virtual Test Bed will be complete with system level visualizations and real-time analysis of the impacts of the PEBB designed.

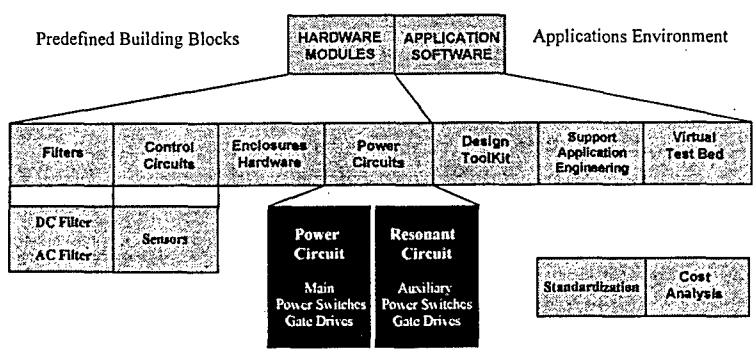


Figure 17. PEBB Parts. The PEBB design and application environment uses CAD tools and predefined building blocks.

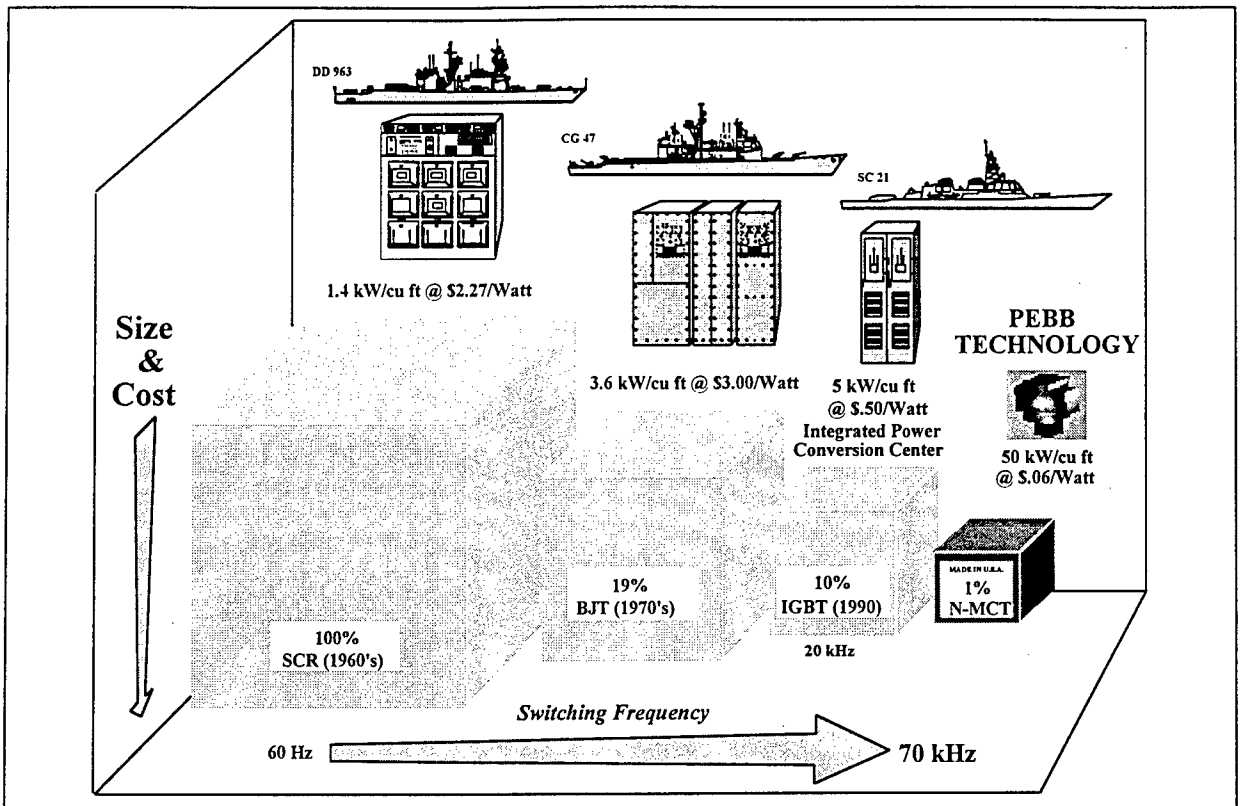


Figure 18. Navy power supply applications are shown with cost and power density referred to Frequency Changers, which use two 3-phase bridges to convert 60Hz to 400 Hz.

An Example, Navy Frequency Changers/Radar Power Supplies

One of the earliest PEBB objectives was to reduce the size, weight and cost of Navy Frequency Changers. Figure 18 shows the original PEBB objectives. Frequency changers are used aboard ship to supply power to power modulator applications like radar, converting 60Hz to 400Hz. Radar loads are non-linear and pulsing. Thus, frequency changers isolate the rest of the ship from the effects of these loads. Radar and aircraft loads are concerned about the quality of power they receive; so, they want frequency changers to isolate them from the rest of the ship power system.

The simplest frequency changer, as stated earlier (figure 11) is made of a converter, an inverter and a DC Link. One PEBB is programmed as a boost converter (rectifier) and the other an inverter. Each PEBB is comprised of power switching, filter and control building blocks.

Status of Cost Reduction.

The 1993 baseline for Navy 250kW inverters is given in Table 2. Compared to this, a rough order of magnitude (ROM) cost was calculated for a 250kW PEBB-1. Zero voltage soft switching is implemented by an Auxiliary Resonant Commutated Pole (ARCP) power-circuit topology. The total cost of the inverter is reduced by 41%. Control cost increased by 33%; however, PEBB controls have increased functionality.

Table 2 Inverter Costs

Inverter Breakouts	Cost (k$)	
	1993 baseline	1996 Pebb-1 ROM
Power Electronics	18	17
Controls	9	12
Filter	36	11
Misc.	27	13
Total	90	53

The significant change was in the filter. The dc and ac filter size dropped from 40% of the machine cost to 22% -- 2/3 reduction of the original filter cost. The added resonant circuit offset these savings slightly. The net result was a 41% cost

saving for the whole inverter and $0.21/W cost factor. Assuming 2 PEBBs, low storage capacitor costs, and no transformer scaling, a frequency changer cost factor would be roughly twice that of an inverter -- $0.42/W in this case.

In the Power Node Control Center (PNCC) project, another PEBB program, SPD Technologies, Barron Associates, IAP Research, and Ingalls Shipbuilding calculate that 35% of the cost of the 400Hz. system on DDG-51 flight IIA could be saved[8]. This is in good agreement with the 41% decrease in inverter cost calculated above. Both of examples show the PEBB program making progress toward cost goals.

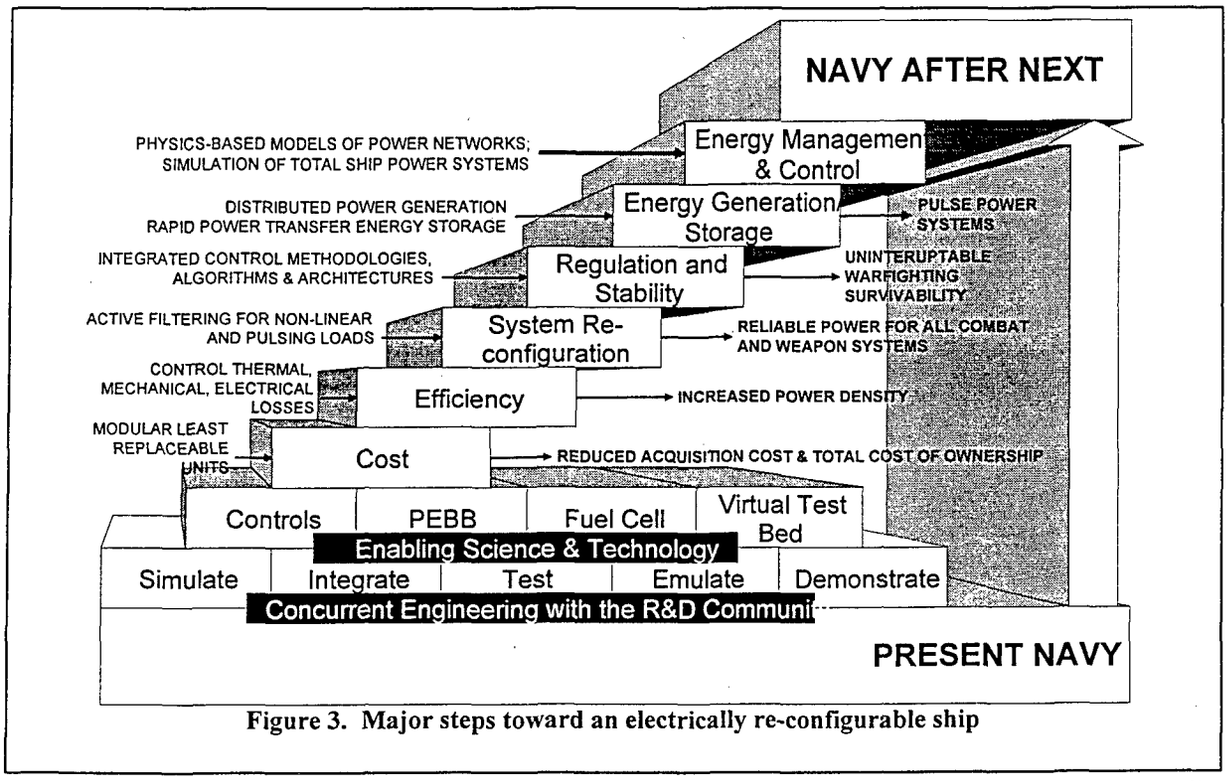


Figure 3. Major steps toward an electrically re-configurable ship

Electrically Re-Configurable Ship

Having reached the Navy's power density and first-cut cost goals, shipboard energy management and control can now be envisioned. Figure 19 shows the major steps toward this future, as planned in ONR's Electrically Re-configurable Ship program. Ship re-configuration has the following meanings:

- Static reconfiguration -- A set of equipment system technologies available for specific configuration for a particular ship, submarine, or aircraft carrier platform. Furthermore, static reconfiguration incorporates platform performance upgrades by means of software and open architecture based equipment upgrades.
- Dynamic reconfiguration -- A platform response to assure power to vital loads during damage or failure. Also, managing the energy from available sources and directing energy to weapons, sensors, armor and propulsion as needed under rapidly changing conditions such as battle.
- Mission reconfiguration – A change in platform state in response to varying readiness conditions such as: cruise, on-station, anchor, battle, etc.

Electric reconfiguration must be realized while controlling cost and reducing manning. Concurrent engineering is essential. Serial science and technology exploration, spanning material through systems, is far too costly and time consuming. As learned in the PEBB program, parallel R&D execution maximizes success and minimizes time and cost. Concurrent engineering management is a nightmare; however, it is the only way to achieve vertical technology integration.

Figure 19 shows the challenges, each building on the other. Cost is basic to all ensuing steps. Beyond acquisition, maintenance, and logistics, costs analysis must become more

sophisticated to weigh technology merits and assess payoffs. Efficiency analysis, particularly heat losses, must yield total ship thermal management strategies.

The frequency changer is an example of the regulation and stability challenge. As stated earlier, ship systems are de-coupled using power supplies and transformers. In the past, a pulse power system would have to provide its own power supply and energy storage so as to be separate from the rest of the ship system. Very quickly size, weight and cost become major factors. If these systems can be "actively" de-coupled, then shipboard systems can be optimized; energy flow can be bi-directional and collectively managed. Conceivably, even the ship's kinetic energy could be harnessed. Advancements in power electronic science and technology will lead to lower cost, more efficient, higher performing ships, submarines, and aircraft carriers.

Acknowledgments

The authors wish to thank the Office of Naval Research and the members of the PEBB team.

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Pebb Toolbox Technologies - Devices to Systems

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Abstract:

The ONR and TRP Pebb (Power Electronic Building Block) program includes a formidable level of concurrent engineering including, at Harris:

- advanced processes capable of high density MOS channels to allow higher peak turn-off currents, particularly in n-type mct's
- large area n and pmct's as well as nigbt's with suitable diodes for application in very high power modules
- compact, low impedance packaging that eliminates conventional wire bonds
- driver IC and integrated gate drive circuit development
- advanced housing, electrical and thermal interfaces that decrease volume and increase performance

All of these developments provide a toolkit of building block technologies that have been demonstrated in several system programs including a 250KW arcp motor drive, now in test at NSWC in Annapolis and a >100KW hard switched Switch Reluctance starter generator intended for aerospace applications. This paper looks at highlights from device, package, driver and inverter viewpoints.

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1. Pebb Toolkit Devices and Device Physics

1.0 Introduction:

The ONR supported Pebb program is intended to revolutionize the way power systems are designed, built and utilized. However, unlike many system programs, it addresses the key power device technologies upon which it is dependent, pushing both MCT's and IGBT's to reach higher levels of conduction and switching efficiencies. Because of particular Navy needs for high frequency power conversion a good deal of the system activity has focused on soft switching circuits, especially the arcp converter, and the devices that best serve those topologies. Our device driven activities have first included advanced processes capable of very high MOS channel density (20 to 30 m/cm2) to allow higher peak turn-off currents, particularly in n-type mct's and second, large area n and pmct's as well as nigbt's with suitable diodes for application in very high power modules. Our system integration of these devices encompasses the development of compact, low impedance packaging that eliminates conventional wire bonds, driver IC and integrated gate drive circuits and advanced housing, electrical and thermal interfaces that decrease volume and increase performance

All of these developments have been realized and demonstrated in several system programs, one of which, a 250KW arcp [1] motor drive, is described in a companion paper while this paper focuses on the basic device issues and includes both device test results and modeling to compare p and n-type mct advantages and disadvantages to n-type igbt's. We first discuss the device limitations and opportunities imposed by MCT and IGBT basic physics. This is followed by some recent n and p-mct pebb device results and finally by modeling results comparing devices built from the same starting wafer with the same carrier lifetime profiles. This is as close to an apples to apples comparison as can be made. The conclusions that are drawn are not unexpected in that they confirm the breakdown voltage (10 to 15%), forward drop (up to a factor of 2) and switching loss advantage of the n-type MCT inherent in its 4-layer structure while shedding some light on the superior controllability of the IGBT that is derived from its series gate control (provided its current is below the latch-up level). To date our system demonstrations have used pmct's, nmct's and NPT nigbt's in the phase leg switches and pmct's as well as a combination of p and n-type mct's in the resonant branches.

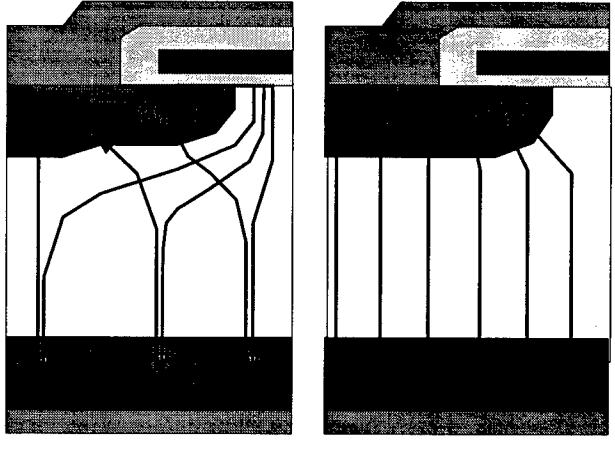
Figures 1 through 4 outline the difference in device physics between the n-type IGBT and the n-type MCT and what that means in terms of ultimate device performance and application. Figure 1 shows their basic cell structures, which are very similar except that the MCT replaces the IGBT's emitter short with a p-channel MOS short. In the SILVACO device simulations that follow figure 4, all junction depths, carrier lifetime profiles and doping profiles are otherwise the same.

Figure 1 also indicates the difference in current flow of electrons and holes which, in the MCT, are typically like a diode, and which, in an IGBT, are forced to separate into a channel portion and an emitter short portion. In most IGBT's the channel portion is most

of the current, leading to a fast device, but obviously puts enormous current, power and thermal stress on the channel. In the MCT channel current flows only during switching leading to a more reliable MOS gate.

Figure 2 shows that the MCT cell structure in real devices is more complicated. Because MCT's latch into the on-state, a single turn-on cell would be enough to turn on the device but, in fact, we design in a high density to enable lightning fast turn-on with no failures even at 175KA/us, our present test limit. The solid circles in figure 2 are the MCT on-FET channels. When we then compare a typical IGBT device of the same channel density as the MCT we see that the shape of the blocking region is quite different in two ways. The small overlap of gate electrode and lower base region of the MCT leads to much lower Miller gate capacitance and much less switching "noise". More important, the shape of the blocking junction leads to near plane junction breakdown voltage in the MCT while the IGBT cell structure's 3-D curvature leads to lower SOA. In our modeling the SOA difference was modest, about 15% higher in the more plane junction MCT.

Fig 1. IGBT and MCT cross sections and current flow lines (MCT requires one additional diffusion)



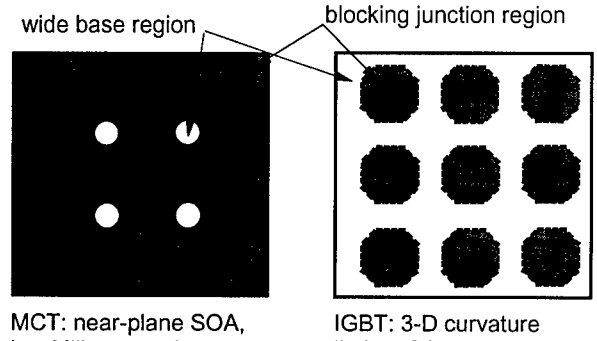


Fig 2. Low MCT on-FET density allows better SOA and Miller capacitance design trade-offs

Figures 3 and 4 look at the basic differences in carrier modulation levels in the MCT and the IGBT that arise because the MCT injects carriers from both sides of the device. Essentially these figures show that the modulated carrier density falls exponentially as one moves away from the emitting junction. In order for 1/e of the carriers leaving the IGBT lower emitter to reach the upper emitter short the diffusion length L must equal W, essentially the thickness of the lower base. This infers a certain level of carrier lifetime, t_h, and, therefor a certain turn-off speed. For a double injection device to have its lowest modulation at an equivalent level, the diffusion length L needs to be only W/2 which can be achieved with a 4 times lower t_h. For this reason we expect, and find, in our simulations that MCT's are both lower in forward drop (better modulation, no JFET or channel contribution to Vf) and up to 4 times faster.

Fig 3. IGBT: Series MOS control, moderate modulation

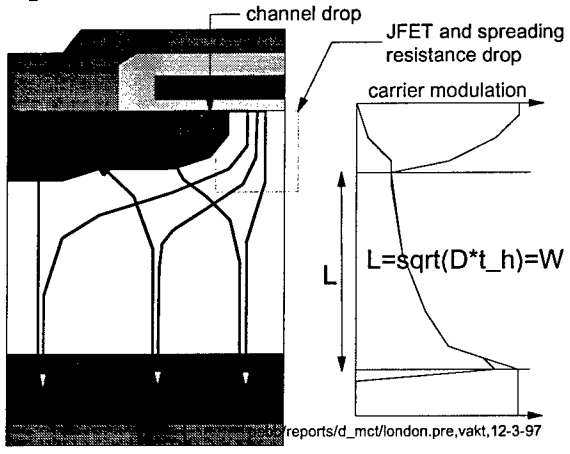
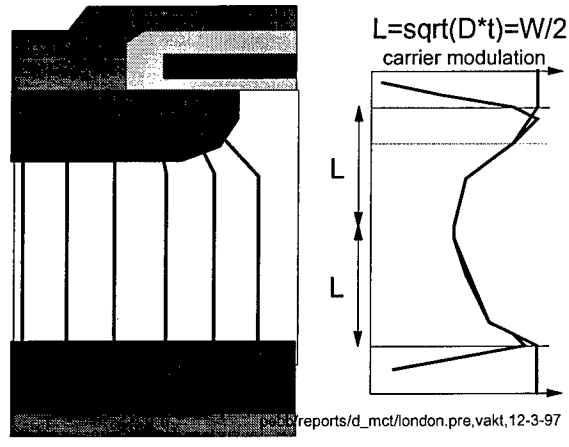


Fig 4. MCT: uniform current, t_rec up to 4 times faster



1.1 Why make a p-type MCT: n vs p-type MCT's

Figures 5-8 are experimental results on developmental n and p-type MCT's. From industry experience with p-type (the blocking voltage primarily supported in p-type silicon) bipolar power devices such as pnp power transistors or p-type IGBT's one would not expect Harris' first MCT product to be p-type. For example, a p-type IGBT is slower with poorer SOA and with a much higher forward drop (the p-channel MOS) than an n-type IGBT. In the MCT speed and SOA are lower than an NMCT but the p-type MCT is still very low in forward drop. The answer lay in the in device cell densities practical 3-5 years ago. The problem with making the n-type MCT was never the vertical device tradeoffs but rather the fact that the off-FET that shorts the upper emitter junction was p-channel and therefor 3 times higher in resistance. Unable to reach off-FET channel densities that would allow us to turn-off 400A/cm2 (for a modest peak controllable current to RMS current rating) at 150C in an NMCT, we thought there would be a market for conduction efficient p-type MCT's at cell densities that were typical in MOS fabs in the early 90's.. That we could and have scaled that p-type MCT capability in the PEBB program is shown by figures 5 which illustrates >500A/cm2 turn-off of about a 1cm2 active area PMCT. Only a few of these devices have to be packaged and paralleled to reach >1000A as seen in fig 6.

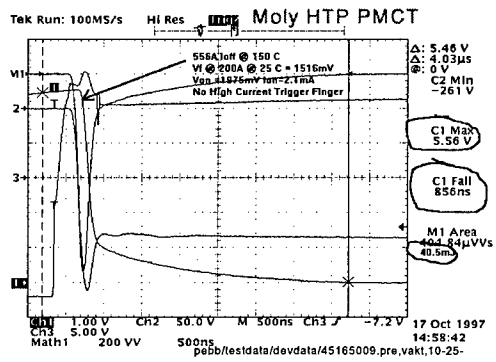


Fig 5. Gen2 PMCT maximum I-off capability >550A/cm2 (150C, 260V)
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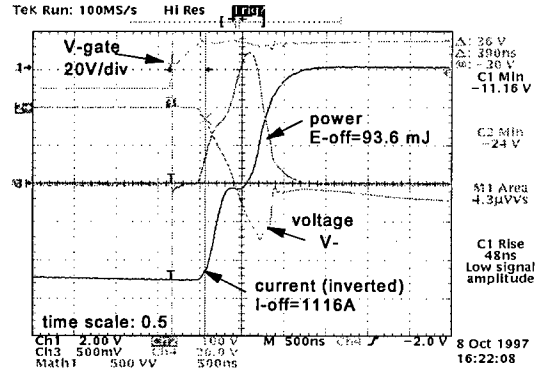

Fig 6. Single switch (3 parallel 600V PMCT HTP's) turn-off at 1116A, 125C
pebb/reports/d_mct/london.pre,vakt,12-3-

During the past 7 years cell densities have increased in order to fabricate low Rds-on low voltage MOSFET's to the point that n-type MCT's can be made that can turn off several hundreds of amperes per square centimeter with simulations projecting reaching 1000A/cm2 I-off levels inside by the end of this phase of the PEBB program. At this time, we have already turned off 1100A/cm2 at room temperature and >500A/cm2 at 150C using a MOS gate density of 25 meters per cm2. Along the way we have been doing our homework, some experimental and some modeling. For example, the experimental device results shown in figure 7 showed the expected improvement in switching speed and forward drop between similar BV n and p-type MCT's while, in figure 8 we show the results of one of our PEBB lot experiments on the effect of the buffer region design (the higher doped region of the lower base of an MCT or IGBT at the lower emitter). The results shown in figure 8 come from hard switched turn-off and forward drop measurements of NMCT's made on two types of starting material and then electron irradiated at various dose levels. The heavier buffer staring material provided many times lower switching loss devices for the same forward drop - repeating results found in moving from first to second generation NIGBT's. The lower loss NMCT's were fabricated in 1200V NIGBT starting material with higher buffer doping.

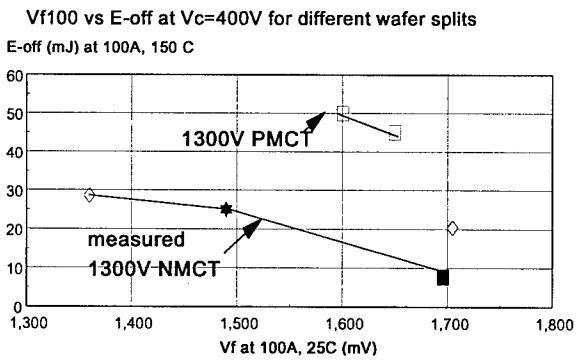

Fig 7. N-type power devices are several times lower in switching losses

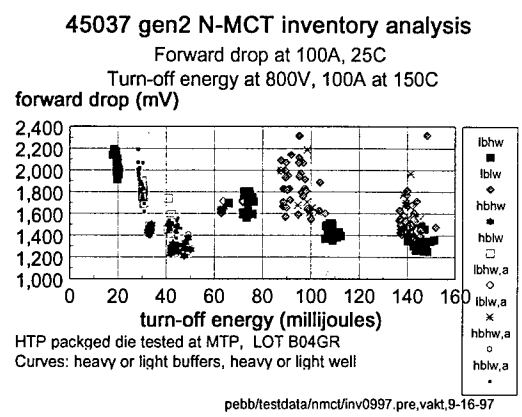

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Fig 8. N-MCT Switching Speed Optimization Experiment
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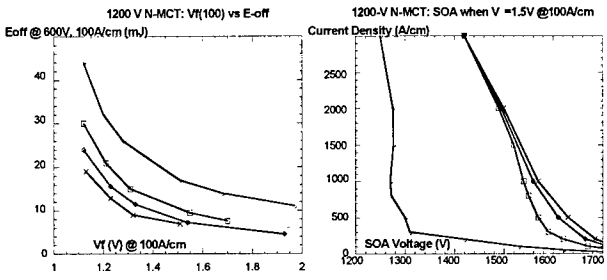
1.2 NMCT and NIGBT simulation study highlights

Figure 9 to 13 outline a simulation experiment on the MCT and IGBT structures, both having the same cell density, 33 m/cm2 (which would make excellent I-off NMCT's and very low channel drop IGBT's), both having the same starting material and the same channel length and both then "electron irradiated" by setting the electron and hole lifetimes in the wide base at different levels (with electron lifetime at 7 times the hole lifetime, presumably the ratio seen using electron irradiation). Each starting material combination of epi thickness (for voltages 300, 600 and 1200V) and buffer charge, 4 levels from 1e13/cm2 to 2e14/cm2) was simulated as an NMCT and as an NIGBT over a complete range of carrier lifetime. For each case a forward drop curve was made and the forward drop tabulated at 100A/cm2. For each case the device SOA was swept out by forcing current at increasing levels with the device held off. Inductive turn-off was at 100A/cm2 at half the device rated BV.

Figure 9 shows, on the left, NMCT results where Vf at 100A/cm2 is plotted on the x-axis against the simulated turn-off energy (both here at 25C) on the y-axis. Each curve is for a 25um thick buffer of increasing doping level. The higher the buffer doping, the better the trade-off. Note, for example, that at about 1.5V Vf the improvement from 1e13 to2e14 buffer is about a factor of 3 much like our experimental result shown earlier. On the right is the SOA for the same buffers. Clearly about a 300v higher SOA is obtained by slightly backing off on the buffer doping to about 1e14/cm2. Note also that, for the SOA curves, we have chosen to pick the carrier lifetime cases with 100A/cm2 forward drops close to 1.5V. Similar curves and data were done for 300V and 600V thick lower bases for the same set of buffer charges for both MCT's and IGBT's and for 25C, 75C and 150C for the optimum buffer case. All results were similar to those discussed below and shown in figures 10 to 13. The 1200V PMCT was also modeled, in this case, by generating an exact device complement of the corresponding NMCT.

Figure 10 is a typical comparison from our study. At these channel densities, 33m/cm2, the IGBT Vf's are extremely low by IGBT standards and NMCT turn-off current exceeds 1000A/cm2. But both the p and n-type MCT's are lower still in Vf because of their much better modulation. And they are lower in Vf despite having a lower t-H (high level carrier lifetime) which simultaneously results in about a 2.5 to 3 times lower switching loss for the NMCT and about the same switching loss for the PMCT. Furthermore, as explained by figure 2 the NMCT is expected to have a higher SOA. For the NMCT point at Vf(100A/cm2)= 1.32V, switching loss=13mJ and the SOA at 1000A I-off was 1560V. In comparison, for the NIGBT point at Vf(100A/cm2)=1.40, switching loss=27mJ and the SOA at 1000A/cm2 is a full 200V lower at 1356V. **This makes the point that the thyristor-based MCT structure is faster, lower in Vf and higher in SOA than the transistor-based IGBT structure with less thermal stress on the MOS channel(s).** This has also been seen in preliminary simulations of more recent vertical structures such as NPT (non-punch-through) structures.

Fig 9. N-type MCT and IGBT Simulation Study to optimize Vf, E-off, SOA at 300, 600 & 1200V

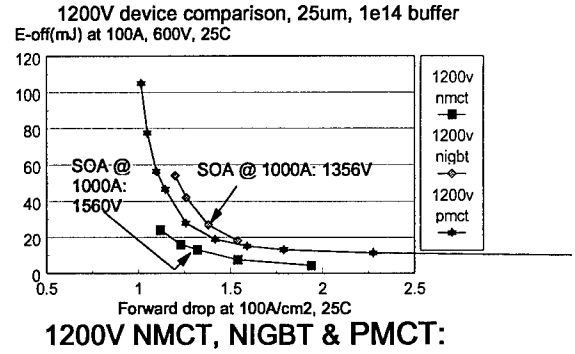


VF vs turn-off loss per cycle (Eoff) for the 1200 V dense channel DMOS MCTs for different buffer Q

Maximum SOAs for the 1200 V 6um-line-cell MCTs vs varied buffer charge for 1.5V Vf@100A MCTs

pebb/reports/d_mct/london.pre,vakt,12-3-97

Fig 10. Switching loss vs conduction loss for nMCT compared to nIGBTs for very dense channel MOS gate:



1200V NMCT, NIGBT & PMCT: E-off vs Vf, 25um buffer

pebb/reports/d_mct/london.pre,vakt,12-3-

What has not been pointed out is the fact that the IGBT's series MOS gate control provides control options that have system value to counter shortcomings in efficiency. For example, over a small but often usable range of gate voltage the IGBT can limit current. This can be put to use in the typical PWM phase leg by moderating the di/dt as current is turned on into say, the lower IGBT from an upper diode thereby lowering the reverse recovery stress on the diode. This is normally done by inserting a properly selected series resistor into the gate circuit, slowing turn-on at the expense of additional turn-on losses but opening diode selection to lower loss diodes. Often quoted IGBT turn-on switching losses are as high as turn-off losses. This turn-on control feature can be built into MCT's as well if two gate terminals are brought out.

IGBT's have another useful control feature arising from the series MOS control. For any give gate voltage and gate threshold voltage there is a channel current at which the channel will pinch off. If the IGBT does not latch up at that current then it will tend to limit current for a short time. The higher the current limit, the higher the dissipation. This dissipation has two components: the component in the several hundred angstrom thick channel given by the current times the gate voltage minus the gate threshold and the overall device dissipation given by the current times the system voltage. As a practical matter the device is able to limit current at perhaps an order of magnitude of current higher than rated RMS current for 10 or 20 microseconds. The current limit of an IGBT with a 5V threshold voltage and driven with a 12 volt gate that had a channel contribution to forward drop of 0.5V at rated current (say, 100A/cm2) would current limit, to first order at (12-5)/.5*100=1400A/cm2. For our 1200V device operating on an 800V buss this would generate an average dissipation of 1.12MW/cm2 in an IGBT silicon volume that could be as thin as 0.015cm for a power density of about 70MW/cm3. At these dissipation levels we have a few microseconds for our controller to decide to turn off the device.

The IGBT's simulated in figure 10 with the unexpectedly low Vf's are possible but they cannot current limit in any useful sense because their channel density, being so high, leads to too low a channel voltage drop. Returning to the simulations that went into the data in figure 10 we found that regardless of the electron irradiation level or buffer charge that the channel drop at 100A/cm2 of device current was between 10 and 12 millivolts. This is seen in the right hand plots in figure 11. A similar low drop of 15 to 24 mV is seen, but plotted for 200A/cm2 for the 600V IGBT's depicted in the left side plots of figure 11. With a gate voltage 5V above threshold (lower is probably untenable in noisy, high current applications) a linear estimate of the channel limited current density is about 50KA/cm2.

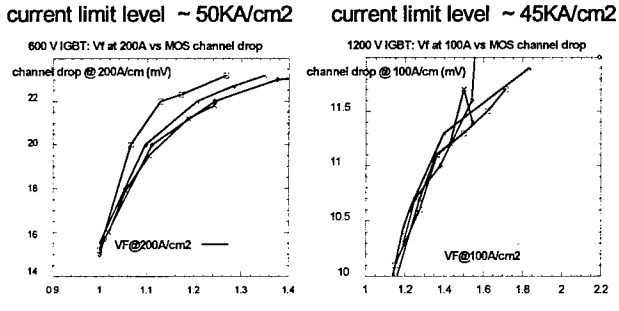


Fig 11. High channel density is a two-edge sword in IGBTs since current limiting capability decreases with increased channel density

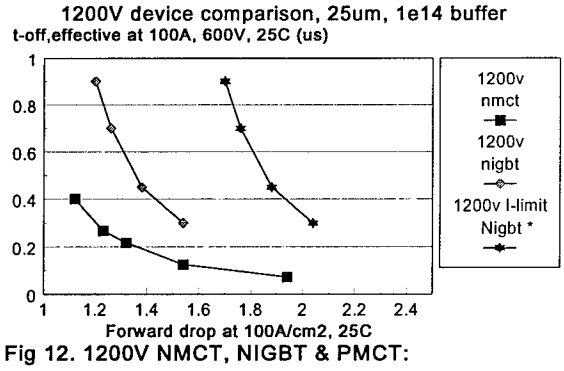


Fig 12. 1200V NMCT, NIGBT & PMCT: t-off vs Vf at 100A/cm2

* assumes 0.5V channel plus JFET drop for current limiting

The conclusion is clear. IGBT's can be designed to be current limiting. If so the high channel densities we needed for 1000A/cm2 maximum turn-off current in the NMCT are not needed **but such IGBT's will have an extra half volt penalty for channel drop under normal operating conditions, so that, at 10 to 20 times rated current the channel will be able to be pinched off. Thus Figures 12 and 13 are then more realistic in NMCT vs NIGBT comparisons as it gives the non-current-limiting as well as a potentially current limiting IGBT switching loss vs forward drop, figure 12 plotting turn-off time vs Vf and figure 13 plotting turn-off energy loss vs Vf.** Note that the data shown was simulated at 25C. Similar results are obtained at higher temperatures.

Simulation limitations: While the simulations above give the best apples to apples comparison of MCT and IGBT one should be careful not to treat the data as etched in stone. First, the calculations are 2-D, not 3-D, which understates MCT conduction and turn-off current capability and overstates IGBT SOA. Second, the specific Vf and E-off curves required assumptions on carrier lifetime distribution and algorithms that, while identical for MCT and IGBT calculations, have some uncertain parameters. Third, both devices will have different curves if different techniques for controlling carrier lifetime are used - for example, platinum doping or neutron irradiation which have already shown up in third and fourth generation IGBT's.

Finally, the structures examined and the few figures from our study shown here were all punch-through designs. In fact, for high voltage devices (>/= 1000V, for example) the best IGBT's, and by inference and preliminary modeling, the best MCT's are produced using a non-punch-through structure with a transparent backside emitter whose function it is to limit wide base transistor gain and to recombine stored charge during turn-off.

1.3 Special MCT designs are practical

Three system related features can be designed into the present generation of MCT's within the process limits of the current generation of PEBB MCT. The first of these is a built-in pilot consisting of a fraction of a percent of the active area cells with a separate power contact. Feeding the current from this contact through a series resistor allows, for resistor voltages up to about 100 mV, a good measure of the entire device current. The current ratio seems to be independent of temperature and fairly linear in this range.

Because the MCT includes IGBT-like cells to turn on the device it is possible to imagine a two-gated MCT that can operate in either IGBT mode or MCT mode.

The third feature is to shift on and off-FET thresholds positive so that device current can be turned off at zero volts. Typically this means shifting the on-FET threshold several volts more negative in an NMCT and shifting the off-FET threshold from several volts positive to 6 or 6 volts negative. We have found in our high current device/module world that bipolar gate drives are common because of the high level of gate noise. However, we have found that system users prefer to have a device that can be powered up in the off-state without power being available to the drive circuitry. Adding a few cells per cm2 in which the emitter is hard shorted accomplished this in the same manner that emitter shorting controlled classical SCR dv/dt capability.

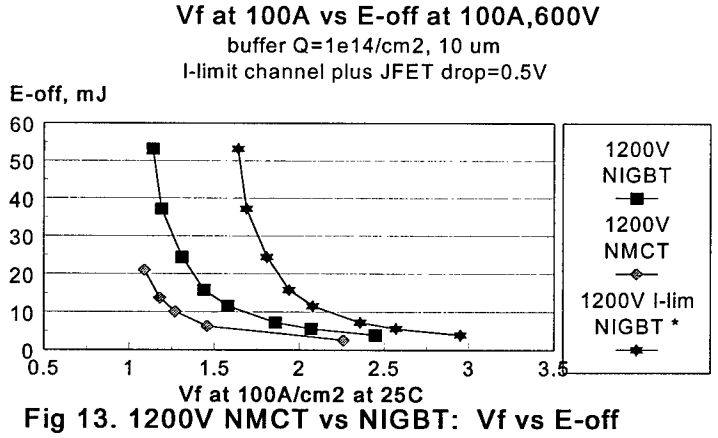


Fig 13. 1200V NMCT vs NIGBT: Vf vs E-off

SOA voltage at 1000A/cm2: MCT 1560, IGBT 1360

*** assumes 0.5V for channel and JFET for current limiting**

1.4 Summary

MCT's are especially suited for low VF and high efficiency while IGBT's can be designed to retain some gate control capability that can be used to soften turn-on and to facilitate a few microseconds of current limiting. MCT's have a higher SOA, much less channel thermal stress and an order of magnitude lower Miller capacitance leading to less switching induced gate noise. Low MCT Vf requires closer matching of Vf's in devices to be paralleled. Low conduction loss and fast MCT turn-on have led to devices with >175KA/us i/dt capability and 45KA peak current (test limits) in a single THINPAK packaged NMCT, an extreme example of the MCT's value in high current applications. IGBT's are a must for applications where random shorts with high di/dt's must be protected against by the power switching device alone. As discussed, these IGBT's must be designed with an appropriate channel drop under normal current operation which degrades on-state efficiency.

2.0 The Thin-Pak, a superior package toolkit technology:

The emerging advanced power device technologies such as Mos Controlled Thyristor (MCT) and (IGBT) are pushing the current densities , switching speeds and frequencies to new dimensions. To fully utilize the capabilities of such devices we need to provide the electrical, structural and thermal environments compatible with their packaging requirements In response to this need, Harris Semiconductor developed the ThinPak technology which offers a new approach for packaging of high performance power devices designed for both commercial and military applications. The ThinPak consists of a power device and a dielectric interposer or simply a lid, with a specific through hole pattern (fig 14a and b). Both surfaces and through holes of the lid are metalized. Since the solderable metalization pattern on the corresponding surfaces of the lid and the die are identical they can be easily soldered together. The power and gate electrodes are then attached to the solderable metalization of the top surface of the lid.

The electrical performance and thermal/structural reliability of THINPAK exceeds those offered by the multiple wire bond alternative. Thermal and electrical characteristics of ThinPak which is an advanced, device level, surface mountable, potentially hermetic package, were modeled and tested. Model and xperimental results are tabulated in table 2. Figure 15 shows one of the module cross sections that was simulated and tested. Note that the integral heat sink provides the maximum performance. Reliability of ThinPak under thermal shock and cycle conditions was experimentally verified.

Fig 14a. Solderable device and lid metals

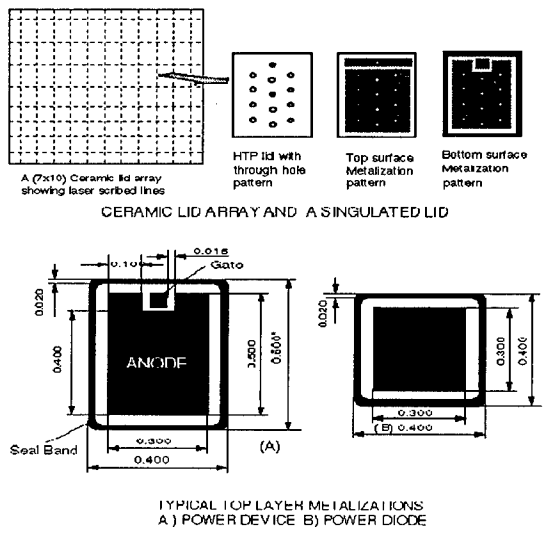


Fig 14b. assembly of a multiple ThinPak

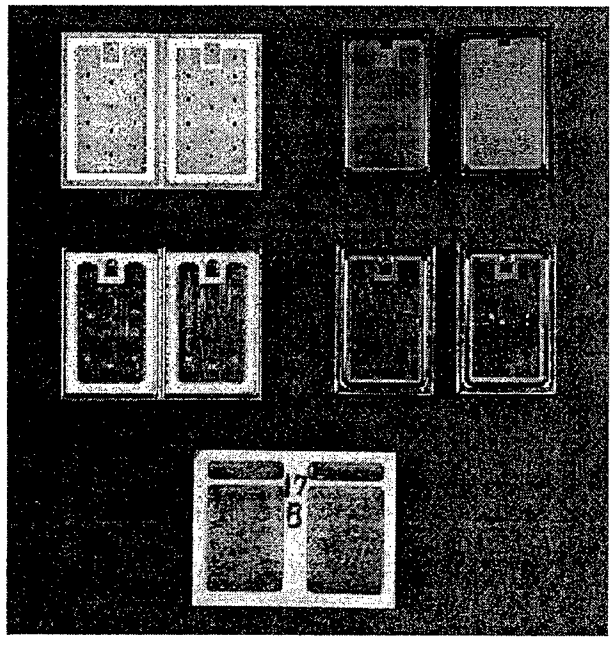
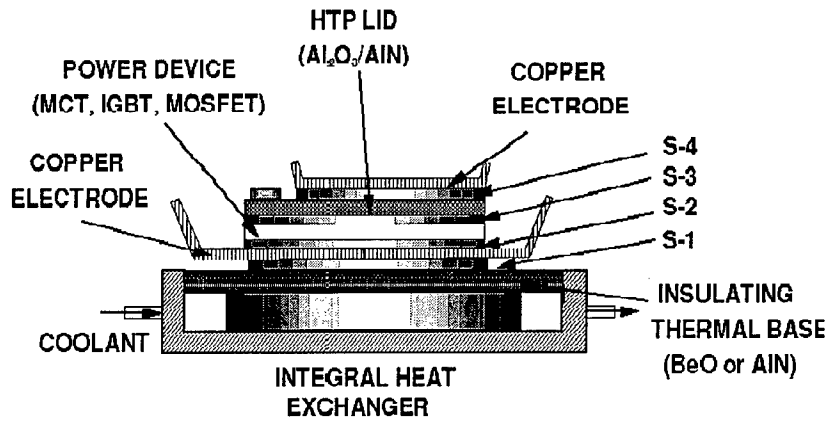


Table 2. Results of 3D FEA for various power module configurations with experimental results from present Pebb toolkit options

	area in2	spreader	heat sink	Tj, calc/expt @ 100W/cm2, active area	Rja, calc/expt	P_60C calc/expt
1	10.2	0.1" AlSiC	external	178/na	.127/na	470/na
2	10.2	0.2" AlSiC	external	163/na	.116/na	515/na
3	10.2	0.2" AlSiC	external	150/na	.107/na	560/na
4	10.2	0.2" CuMo	external	147/na	.105/na	571/na
5	10.2	0.2" CuMo	external	129/na	.092/na	651/na
6	10.2	0.1" CuMo	external	164/na	.117/na	512/na
7	10.2	0.1" CuMo	baffled	121/na	.086/na	694/na
8	10.2	0.1" CuMo	integral 40%Cu40	70/na	.050/na	1200/na
9	10.2	0.15" Cu	external	137/na	.980/na	613/na
10	3.1	none	external	264/94C@500W	.189/.19	318/320
11	3.1	none	baffled	162/80C@800W	.116/.10	519/600
12	3.1	none	integral 40% Cu40	60/55C@1000W	.043/.055	1400/1100
13	3.1	none	integral 40% Cu10	na/100C@2000W	na/.05	na/1200
14	3.1	none	integral 40% Cu	na/65C@1000W	na/.065	na/925

Fig 15. Module Stack Elements



3.0 Control toolkit technology, the "driver2 IC"

The performance limits of today's MOS controlled power devices has quickly and steadily increasing over the past two decades. Device performance of the IGBT (Insulated Gate Bipolar Transistor) has grown from a meager 1 Amp, 200 volt very fragile device to a cornerstone component that is regularly called on to control currents in excess of one hundred amperes and voltages in the range of 600, to 1600 volts. MCT's (MOS Controlled Thyristors) have also reached similar levels of voltage and somewhat higher levels of performance in terms of current and current density. EST's (Emitter Switched Thyristors) will also dwell in this high power domain. Additionally, power MOSFET's have grown in active die area to exceed 1 centimeter square. These are all substantial devices with applications that make use of their individual attributes; however, their development has also required the development of new gate drivers that are very fast and rugged.

What is presented is a family of gate drivers that are intended to address the needs of high power MOS gated devices. In the case of the MCT the gate capacitance is simply the equivalent of a parallel plate system, for an active area of 1 sq. cm. the gate capacitance is typically on the order of 40nF. However the situation is somewhat more complex in devices that exhibit a more pronounced Miller Effect, as with IGBT's and MOSFET's. In the case with these devices, the Miller Effect works to effectively increase the total charge that must be supplied by the gate driver. The requirements of a gate drive circuit that must reliably control these devices is fast rise and fall times, with excellent slewing capabilities with capacitive loads, both linear and non-linear. As a result of the capacitive nature of the gate, the peak currents developed can be quite high. In the case of an MCT

gate being driven from -15 volts to +15 volts, in 100 nanoseconds an estimate for the charging current of 12 Amperes per sq. cm. of active device area is typical.

The family of gate drivers we have developed and tested is built around an IC (integrated circuit) shown in figure 16 using a Power BiMOS process. In its simplest form it is provided as a single IC in a 28 pin surface mount plastic package. A three die version which includes two discrete MOSFET's as an power amplifier is also packaged in the same 28 pin surface mount plastic package. Performance Data is presented as well as an actual high power inverter application. A final main option includes the driver IC and a charge pump to satisfy applications which require both gate drive polarities without the user having to provide a special power supply. The output impedance of the non-amplified versions is sufficiently low to serve most applications.

Table 2: General Driver Specifications		
Rise and Fall Time	80 -160	nseconds
Programmable Propagation Delay	0.14 - 10^5	μseconds
Output Swing (pk-pk)	30	volts
Output Current Peak	2 - 44	amps
Load Capacitance	4 - 180	nF
Load Impedance	0.1	ohm

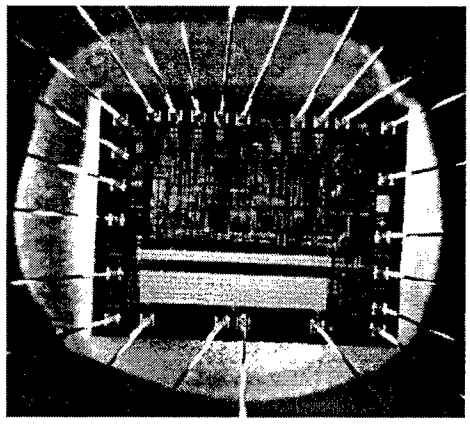


Fig 16. "Driver2" IC

Features

Programming for either polarity of power semiconductor,
Unlatched or latched operation using synchronous or asynchronous clocking,
Temperature sensing of the IC, with a flag set at a nominal 165 C,
Undervoltage sensing and lockout,
Auxiliary +/- 5 volt power supplies,
Auxiliary comparator switching < 100 nanoseconds
Auxiliary op amp > 750 kHz bandwidth

4.0 250KW Soft Switched ARCP Inverter Demonstration

The effort of providing a more integrated, modular design of power electronic systems by employing advanced power semiconductor devices and advanced packaging technologies as well as more standardized control interfaces leads to the Power Electronics Building Block (PEBB) concept. This section will focus on one design example for a PEBB application, a 250KW soft-switching inverter with 20KHz operating frequency. An

Auxiliary Resonant Commutated Pole (ARCP) topology [1] is chosen to achieve zero-voltage switching for both turn-on and turn-off of the main power devices. Auxiliary switches are MOS Controlled Thyristors (MCT's) because of their high peak current handling capability [2] and high di/dt and high dv/dt capability. N and p-type MCT's allow the auxiliary switch gate drivers to be referenced to a stable operating point, simplifying auxiliary switch control and increasing reliability. The Thin Pack technology [3] is used to eliminate wire bonding ensuring low inductance design and more uniform dynamic current distribution. The pebb device modules include an advanced integrated fluid heat exchanger that more than doubles the total heat removal efficiency from the power silicon junction to the cooling liquid. Detailed design calculations based on optimized space vector modulation and ARCP operation provide the high frequency performance of the inverter including the total harmonic distortion (THD), RMS ripple current through the DC bus capacitor, and the RMS current carried by the laminated bus bars. With actual measured data of the power silicon devices, the total dissipation of the main and auxiliary switches is calculated which leads to a decision of choosing enough silicon dies in parallel to match the allowable heat flux in this design. The mechanical design emphasizes low material and assembly cost and provides options for lower power, modular packages with minimum modifications of physical dimensions. The gate driving circuitry provides tight and balanced gate signals to all the semiconductor die. Special detection circuitry is included to achieve zero voltage switching under various load and line conditions. The inverter is being built up to deliver its full power capability. Preliminary experimental results are presented.

4.1 Brief System Specification

The inverter is a voltage source type with resonant circuitry to soften the switching edges. It has a 750V DC input and 450VRMS three-phase output. The load power factor is inductive (0.85) for a peak output power of 250KVA. Space vector modulation will be used to maximize the voltage conversion ratio and to cut down the switching losses. The modulation depth will be 85% to leave enough room for soft switching commutation.

4.2 Inverter Topology and Design Consideration

The ARCP topology [1] is shown in Figure 17. The main switches are configured as regular half bridge with the resonant capacitance right across them. At the turn-off of the main switches, the resonant capacitors act as snubber capacitors which reduce the turn-off losses. At the turn-on, the energy stored in resonant capacitors are recycled through the resonant commutation in a loss free manner. Meanwhile, the current in the freewheeling diode is softly commutated and the main switch is turned on under a zero voltage condition. The auxiliary switches are configured as four quadrant AC switches with two independent gate controls. The AC switch is operated under zero current switching conditions, which makes MCT's ideal candidates for this application.
The design of the resonant components depends upon several factors which are:

- turn-off speed of the main switch;

- maximum allowable loss of the duty cycle because of the resonant commutation;
- the amount of circulating energy through the auxiliary circuit; and
- the timing resolution of the control circuit.

The first design consideration is to minimize the main switch turn-off loss plus the circulating energy loss. This leads to an choice of optimal resonant capacitance. The resonant inductance then determines the loss of the duty cycle with the chosen resonant capacitance. Keeping the maximum duty cycle to be about 90% in this design, the resonant inductance should not be too small otherwise the di/dt will be too high which can cause too much reverse recovery loss in the AC switch and makes the control timing more difficult. In this case, the propagation delay of the gate driving circuits and the storage-time of the bipolar power switches need to be carefully included.

The current design uses 1400V non-punch through (NPT) IGBT's as main switches. These are Harris developmental devices. The IGBT's have fast turn-off speed (see next section for details) which makes 400nF resonant capacitance a right choice. The resonant inductance is chosen to be 1.2uH based the discussion above.

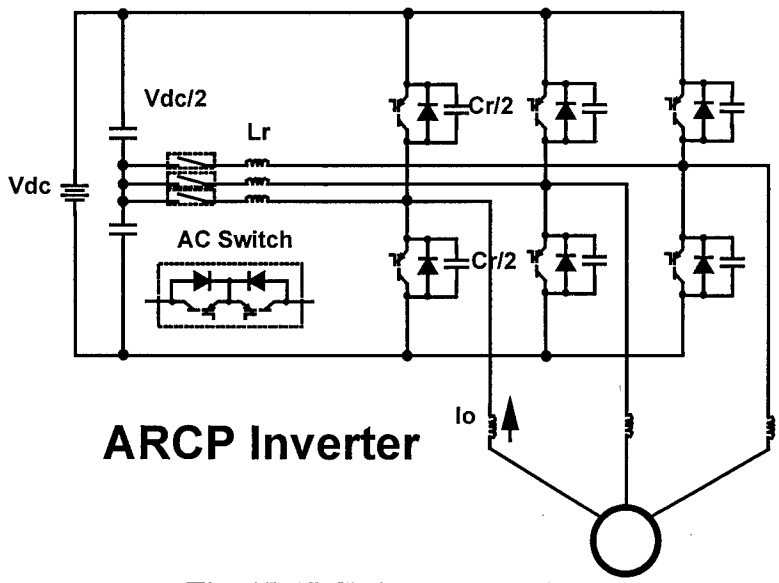
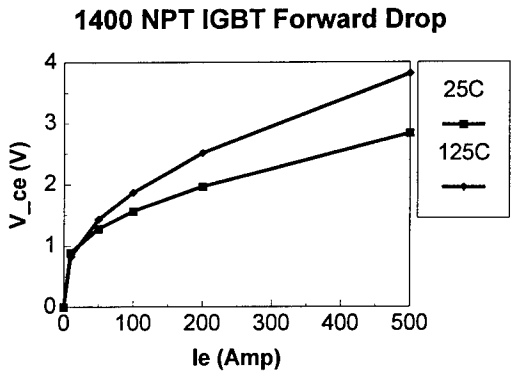


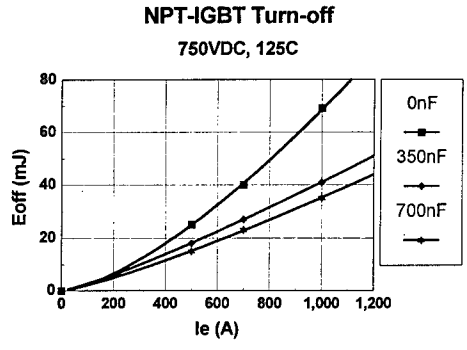
Fig. 17 ARCP inverter topology.

4.3 Characterization of Power Silicon Devices

The test results of a Harris 1400V NPT IGBT are shown in Fig.18. The data provide the basis for choosing the resonant capacitance and the basis for scaling the number of die per main switch.



[A]



[B]

Fig. 18 Test results of Harris 1400V NPT-IGBT.

4.4 Inverter Performance and Power Dissipation

For this specific application, the total harmonic distortion (THD) of the inverter output needs to be low. With space vector modulation and assuming a second order filter is used to remove the switching frequency harmonics, the THD can be calculated for different switching frequencies, as shown in Fig. 19. A typical spectrum of the phase to neutral voltage before and after filtering is also shown in Fig.20 .

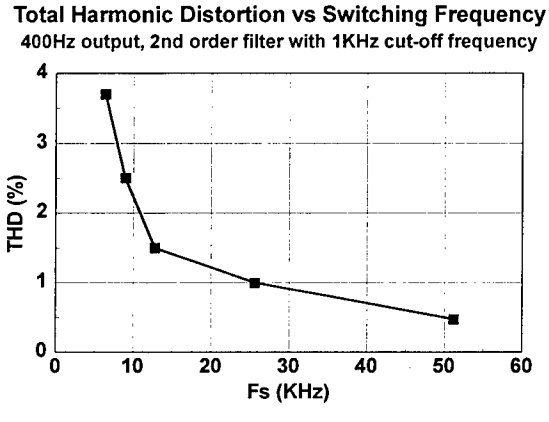


Fig. 19 Inverter output THD vs. switching frequency

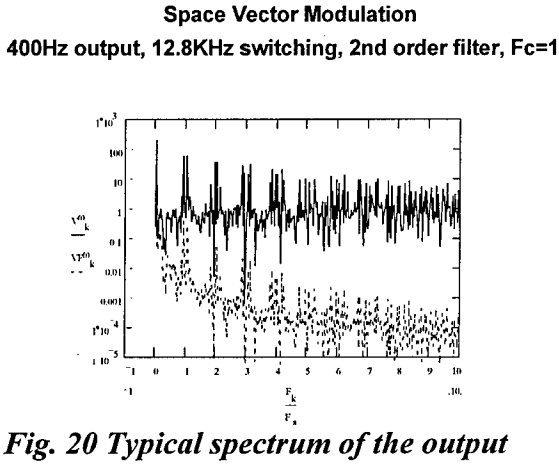


Fig. 20 Typical spectrum of the output phase to neutral spectrum before and after filtering

Using the test data of the power devices, the design parameters and the dissipation in the power devices can calculated. The following assumptions are used in our calculations:

• Vdc=750V • Vac=450VRMS • Po=250KVA • PF=0.85 • Peak Current=453A • Modulation Depth=0.85 • Modified Space Vector Modulation • Fs = 20 kHz • Variable Boost ARCP (Lr = 1.2 uH)	• I_boost / I_r_peak = 0.5 • Main Switch = 4 Size-8 IGBT + 4 Size-7 Diode • AC Switch = 1 Size-8 MCT + 1 Size-7 Diode • Device Type: Phase Switch: Harris 1400V NPT IGBT Phase Diode: Harris 1400 low forward drop AC Switch: Harris 1200V PMCT and NMCT • AC Diode: Harris 1200V fast reverse recovery

The results of the calculation are shown in Table 3. It can be seen that the low forward drop and the low conduction duty make the diode conduction loss very low. By doubling the resonant capacitance, both the switching losses of the main switch and the AC switch increase because of the excessive ARCP boost operation and the higher circulating energy level. As a result, the AC switch dissipation and RMS current of the resonant inductor increase significantly, which can easily cause overheating in the resonant circuitry. Please also notice a significant amount of the ripple current flows through the DC capacitor bank and this will dictate the DC capacitor design if electrolytic types are chosen.

Table 3 Loss calculations	Cr= 400nF	Cr= 800nF
IGBT Conduction Loss per Main Switch (W)	393	393
Diode Conduction Loss per Main Switch (W)	26	26
Averaged IGBT Switching Loss per Switching Cycle (mJ)	4.8	5.05
Averaged AC Switch Loss per Switching Cycle (mJ)	5.9	8.37
Peak Resonant Current (A)	755	903
RMS Resonant Current (A)	78	111
Total Main Switch Losses (W)	3123	3154
Total AC Switch Losses (W)	660	990
AC Switch Snubber Losses (W)	318	352
RMS Current of DC Bus Bar (A)	329	329
RMS Current of DC Capacitor Bank (A)	177	177
Inverter Efficiency (%)	98.0	97.8

As a comparison, the switching losses of a hard switched inverter using similar kinds of power devices will be much higher as shown in Figure 21. In general, soft-switching technologies can greatly improve system performances:

⇒ Higher switching frequency:
⇒ Smaller filter components;
⇒ Less total-harmonic-distortion (THD);
⇒ Better dynamic response - wider control bandwidth;
⇒ Lower EMI.

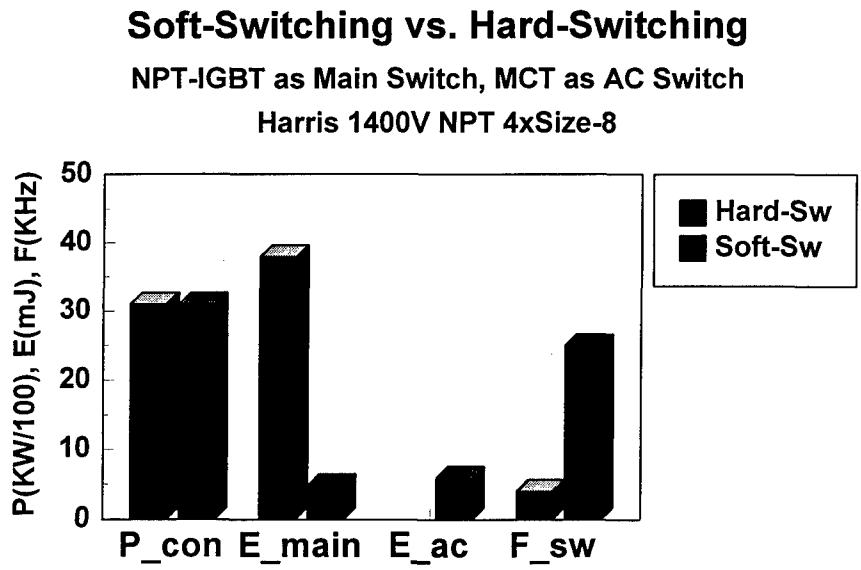


Fig. 21 Comparison of hard switching and the soft switching.

4.5 Utilization of ThinPak Technology

The HTP package is employed in this design to eliminate wire bonding of the power devices. The HTP device, shown in Figure 22, allows direct soldering of the power electrode to the top of the silicon device. With HTP's, low inductance design of the power package is facilitated and current handling capability is increased over the traditional wire bond package.

To improve the heat removal capability, an advanced heat exchanger technology is employed in this design which has a benchmark performance of 60C junction to cooling water temperature rise for a 250W/cm2 heat flux under 1GPM flow rate. This low cost, compact technology greatly improves the thermal bottom line of the entire inverter. The package used for an ARCP inverter leg is shown Figure 23. Three of these legs will form a three phase inverter.

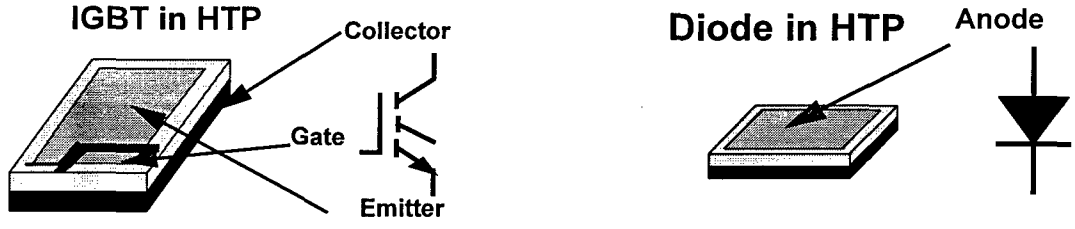


Fig. 22 ThinPak packages reduce inductance design and increase current capability.

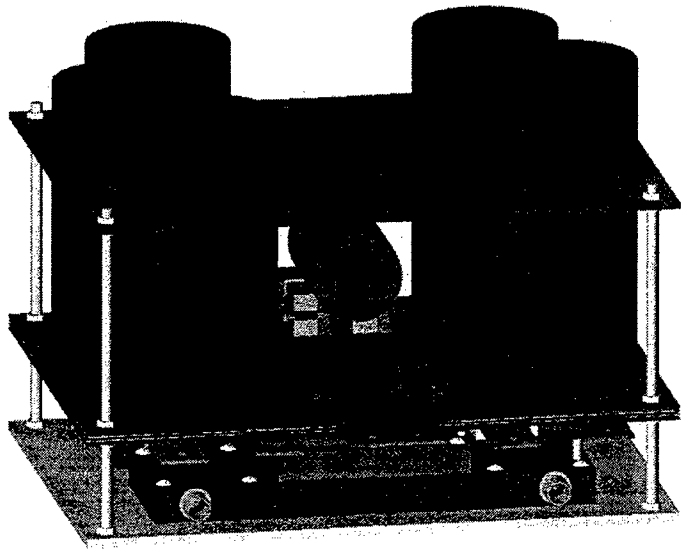


Fig. 23 ARCP inverter leg package (courtesy NSWC system team)
Note that the Harris activity was responsible for the Pebb ARCP leg shown above up to, but not including, the bus structure. Test data shown in this paper is from single leg tests.

4.6 Sample Experimental Result

Currently, the inverter is under quarter power test. The waveforms in Figure 24 show the unit doing single pulse ARCP operation under 800V DC bus condition and the main switch turning off 300A of load current. The low inductance design of the power module, the soft-switching operation, and laminated DC bus structure are the contributing factors to have the overshoot voltage well under control. More tests will be conducted in the near future and the results will be presented.

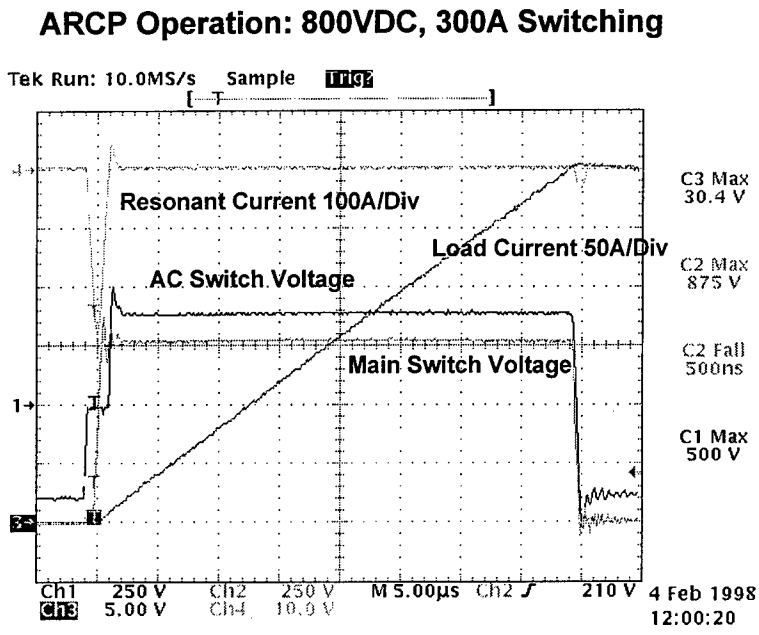


Fig. 24 ARCP leg operation: 800V dc bus; main switch turns off 300A.

4.7 Summary

A soft-switching three-phase inverter using ARCP topology is designed. The goal is to deliver 250KW of output power with 20KHz carrier frequency. To reduce the power dissipation, fast NPT IGBT's are used as main switches and p-type and n-type MCT's are combined in the auxiliary switch to best utilize the strength of these devices. HTP packaging technology provides opportunities for low inductance design and better current handling capability. A more efficient heat exchanger improves the thermal bottom line of the whole system. The electrical, thermal, and mechanical considerations are combined leading to the final design of components and the inverter assembly. System performance and efficiency are projected based on detailed calculations with parameters derived from device and ARCP leg testing. The complete inverter is currently being tested at ¼ power level at NSWC.

5. Conclusion

The material presented has illustrated some of the scope and the capability of the device, package, gate drive and assembly toolkit being developed to support Power Electronic Building Blocks. This is clearly demonstrated in the example of the NSWC 250KW ARCP inverter which includes toolkit n and p mct's, n-igbt's and diode, advanced packaging and cooling concepts along with toolkit elements to simplify gating and control.

Acknowledgments:

The authors of this paper wish to thank ONR for its support of the PEBB program under which much of the work reported above was done in particular, Terry Ericsen, the ONR program manager, and Joe Borraccini, Bill Ruby, and their team at NSWC, Annapolis, for their guidance and support.

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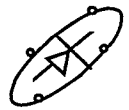
2. Temple and E. X. Yang, "MOS controlled thyristor switches," Proc. PCIM PowerSystems World'97 Conference, Baltimore, 1997
3. Ozmat, V.A.K. Temple and J.K. Azotea, "An Advanced Packaging Technology for High Performance Power Devices" AICE Proceedings of the 32nd Intersociety Energy Conversion Engineering Conference, July 27 - August 1, 1997, pp 694-699



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HPEBB OVERVIEW

by

H. Mehta

***S*ilicon *P*ower *CO*rporation**

Malvern, PA

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Mission

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'To Serve the Global Power Electronics Market with Leading Edge Components and Systems Offering Optimum Value and Quality to Our Customers'

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Power Electronic Systems

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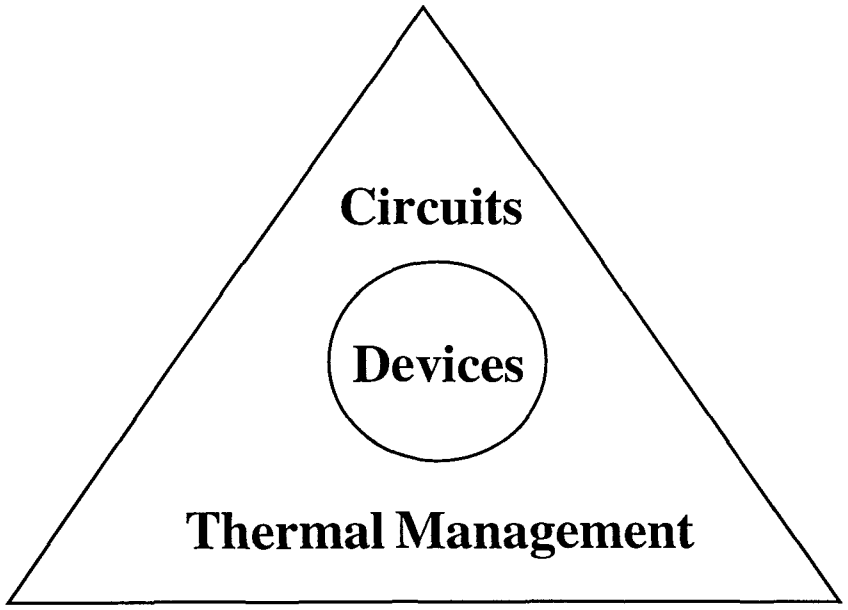

Key Ingredients :

- Semiconductor Devices
- Control & Auxiliary Circuits
- Thermal Management Packaging

Applications :

- Power Conditioning
- Conversion

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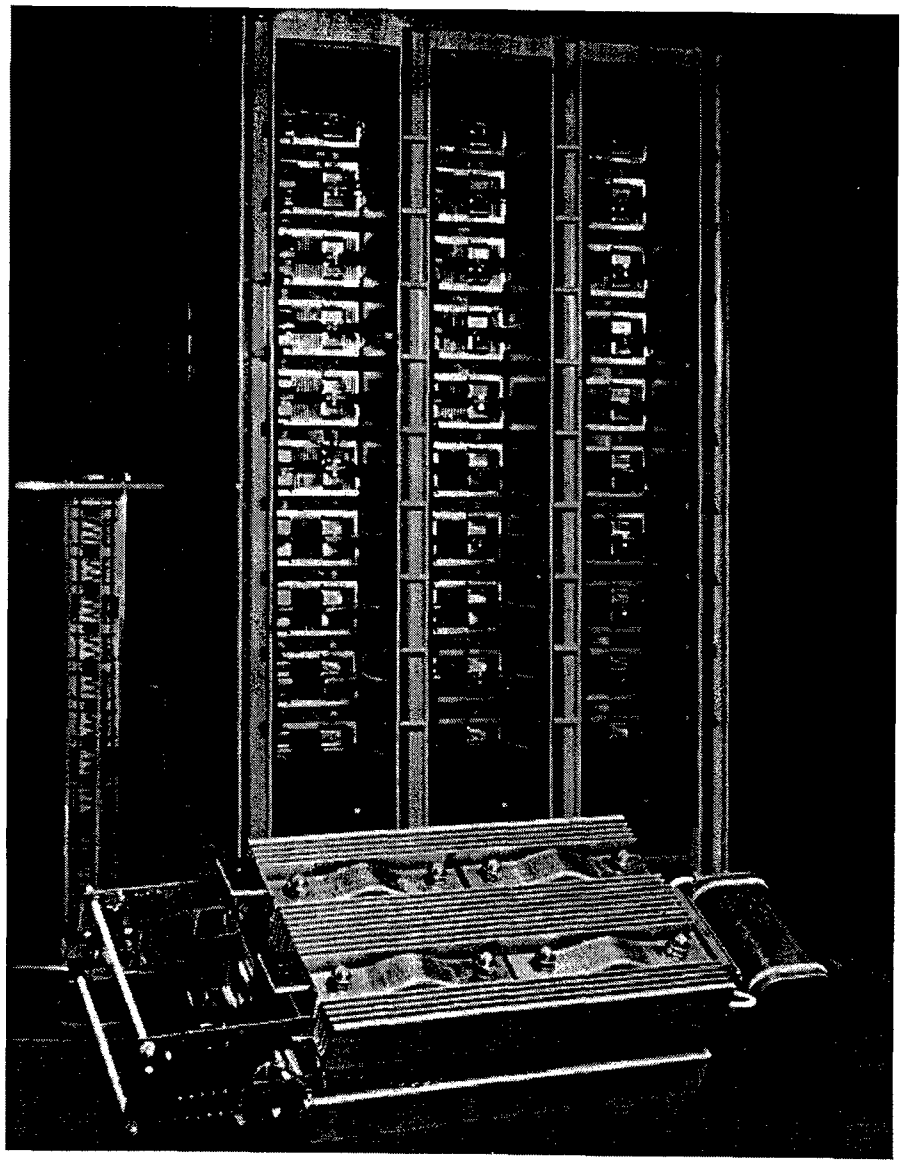

Challenge

- Size, weight, cost reduction
- High availability, reliability, maintainability

Response

- Continue to push technology and manufacturability envelope (size, weight)
- Aggressive product-based approach
- Innovative modular system-volume, reliability

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Product Applications

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Heavy Industrial

- Induction Heating, Aluminum Smelting, Chlorine
- Metal Rolling, Large Pump & Fan Control
- UPS Oil Well Drilling

Transportation

- Locomotives, Rapid Transit, Off-Highway Vehicles

Electric Utility

- Static VAR, Turbine Excitation, Custom Power
- Thyristor Controlled Series Compensations (FACTS)

Military

- Navy : PEBB, Nuclear Controls
- Army : Electric Gun Programs (EM & ETC) & Pulse Power

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SPCO Qualifications

- manufacturer of high voltage & high current electronic devices
- new power electronic devices with high ratings
- soft-switching inverter technology
- converter and system control technology

SPCO Products

- high quality SCRs, diodes up to 9,000 V
- light-triggered thyristors up to 8,000 V
- GTOs up to 6,000 V
- new 125 mm SCR 6 kV, 4.0 kA
- new 100 mm GTO 6 kV, 3.0 kA
- new 53 mm MTO 9 kV, 1.2 kA
- generic power modules (SCR, MCT, MTO)
- high power inverters from 100 kVA to 10 MVA for APF, Drives, STATCON, PS & UPS

SPCO "The Power Electronic People"

- specializes in high quality, high power electronic products
- supplier of power electronic devices and systems for utility, industrial & military customers

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SPCO Process Chain

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Stage 1 - Components

Advanced Packaging

- Structured Copper
- Plastic Package
- High Temp. Package

- Present Thyristors (77mm)
- Larger Thyristors (100,125mm)
- MOS Turn-Off Thyristor
- SiC MTO Thyristor
- Advanced MTO Thyristor

Stage 2 - Systems

- Power Processors
- Pulse Power Switches
- Static Voltage Regulators (SVR)
- Static Transfer Switches (MVSTS, LVSTS)
- STATCON / UPS

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HYBRID MTO™

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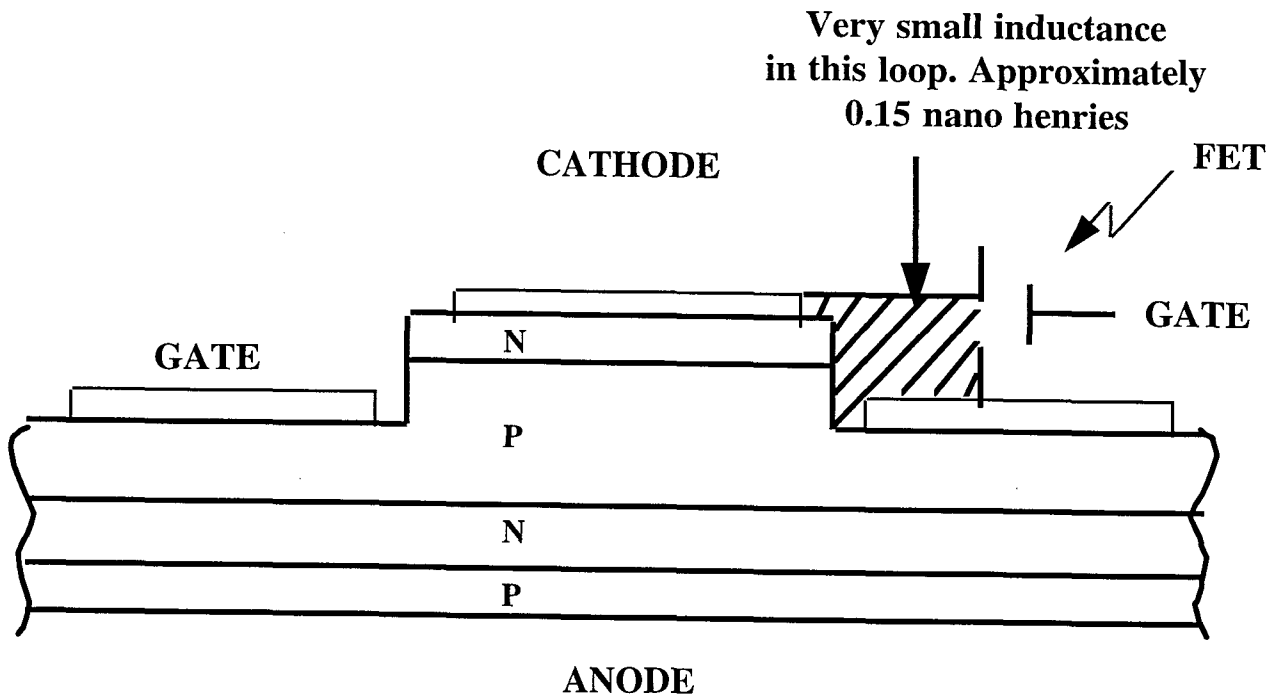
(PATENT # 5,005,065)



By putting the FET in a low resistance state, the current by passes the emitter junction and the device turns off with unity gain

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MTO™ THYRISTOR STRUCTURE

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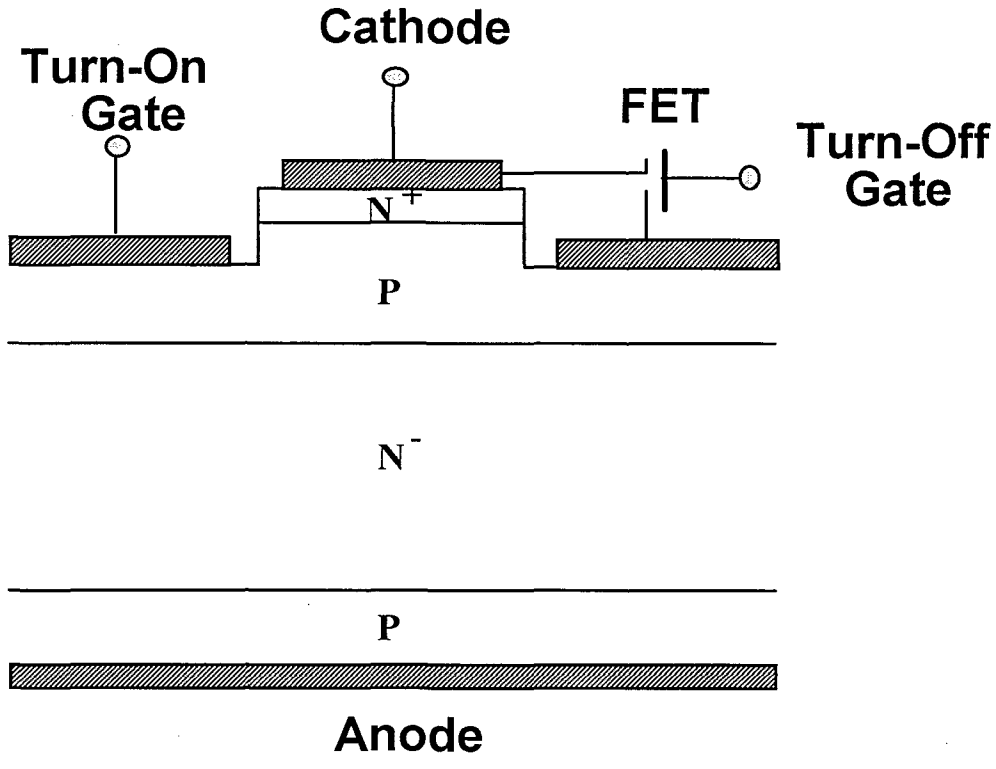
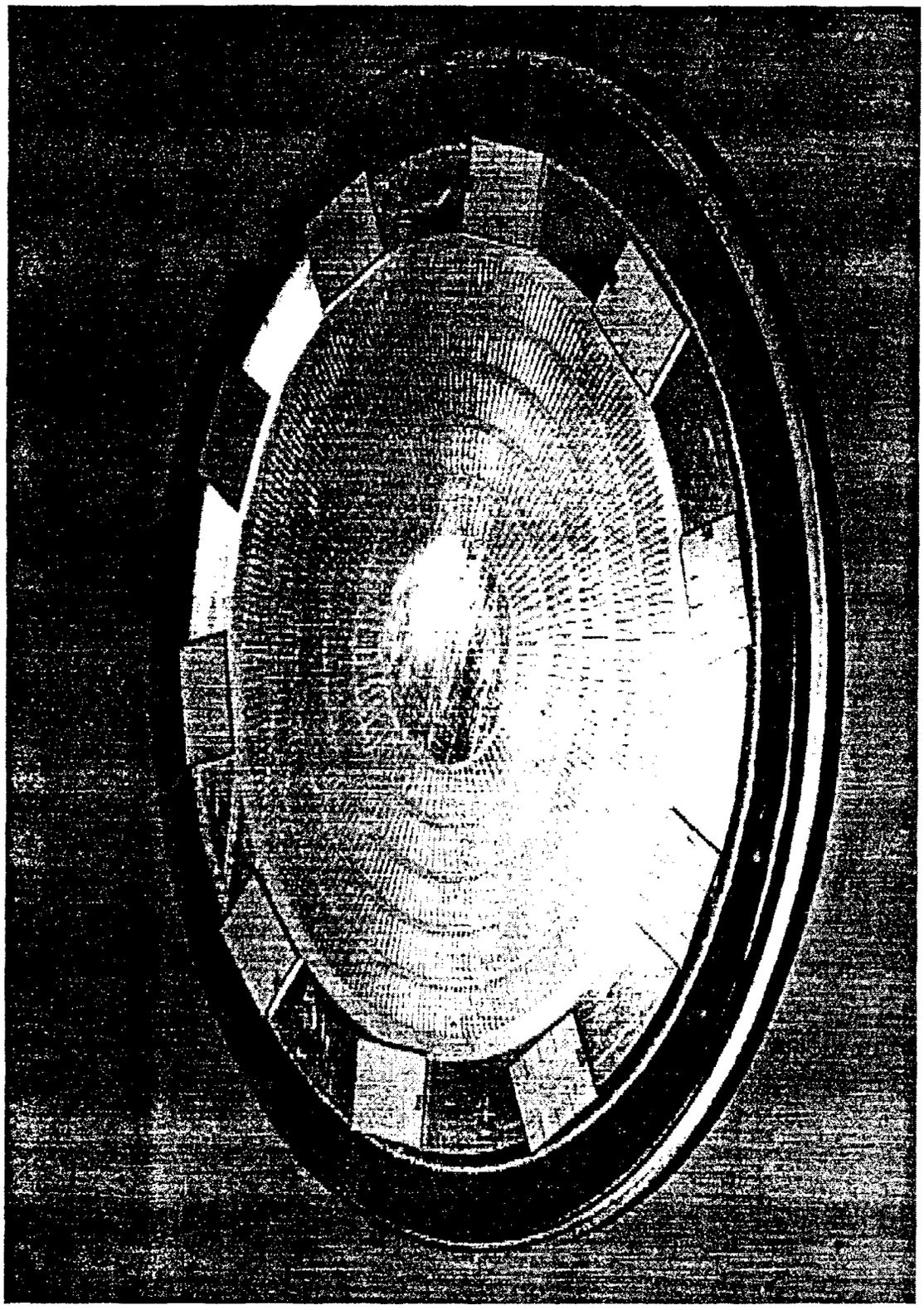


- TURN ON WITH NORMAL GATE
- TURN OFF WITH FET GATE



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MTO™ THYRISTOR ADVANTAGES

ISO 9001 Certified

- **Short storage time (1 - 1.5 micro sec)**
  - ⁕ series operation
- **Not voltage limited**
  - ⁕ 9kV demonstrated
- **Gate drive advantages**
  - ⁕ Fewer parts count
    - lower volume
    - lower cost
    - higher reliability

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MTO™ Operation

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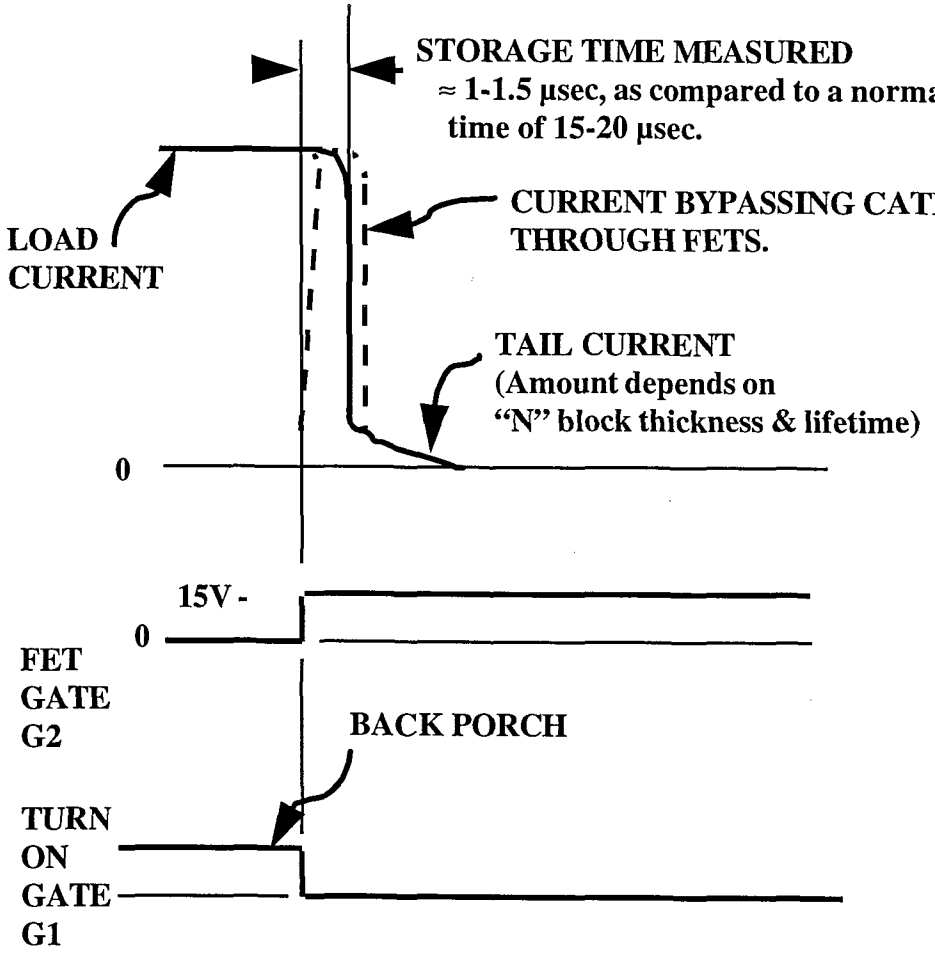

GAIN = LOAD CURRENT / CURRENT BYPASSING CATHODE

NOTE : Gain equals unity during storage time and exceeds unity during fall time because of a slight lag in the bypass current due to small inductance in FET cathode loop.

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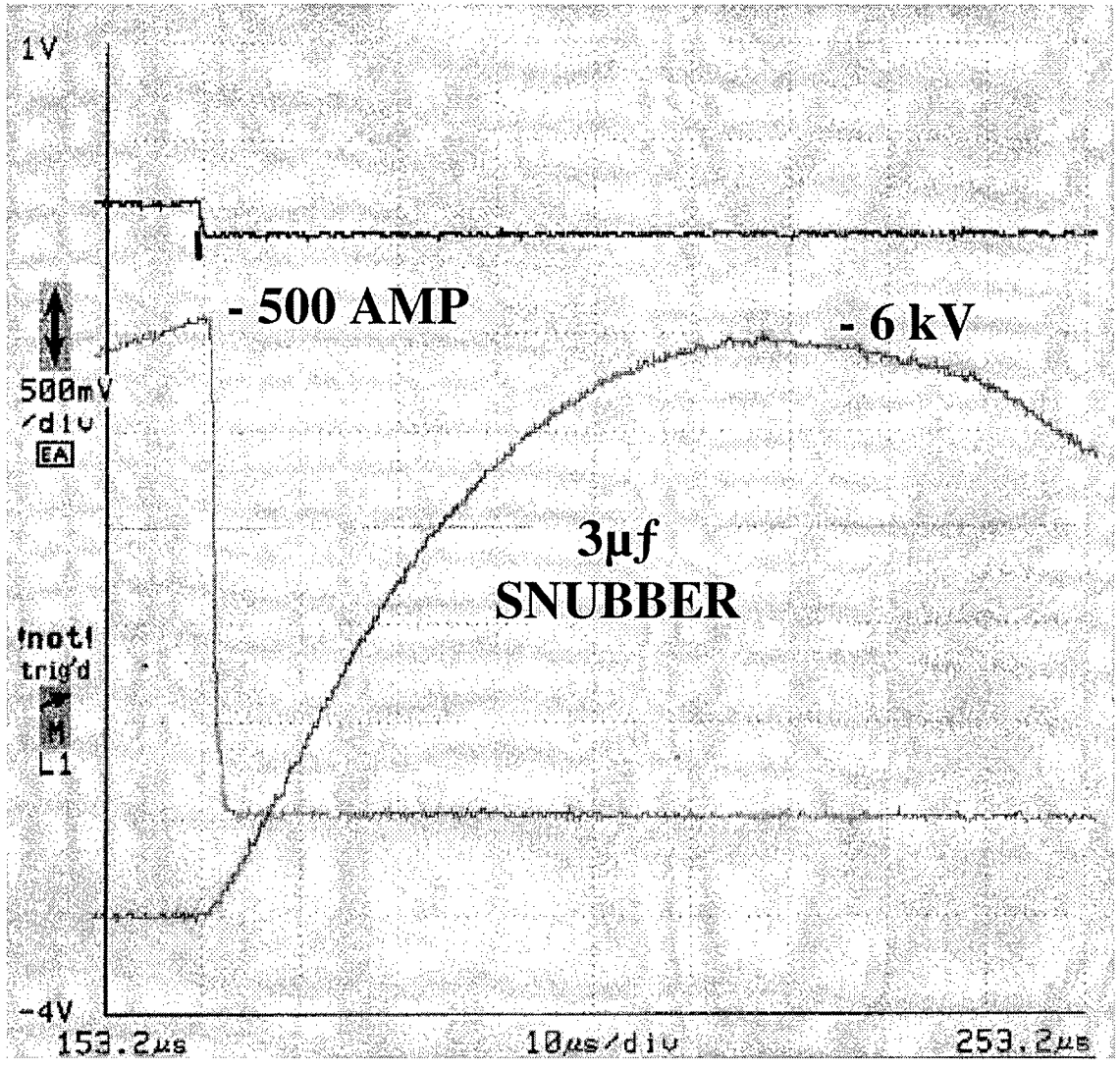
MTO™ 1431-3A
9kV

ISO 9001
Certified



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2800 V MTO™

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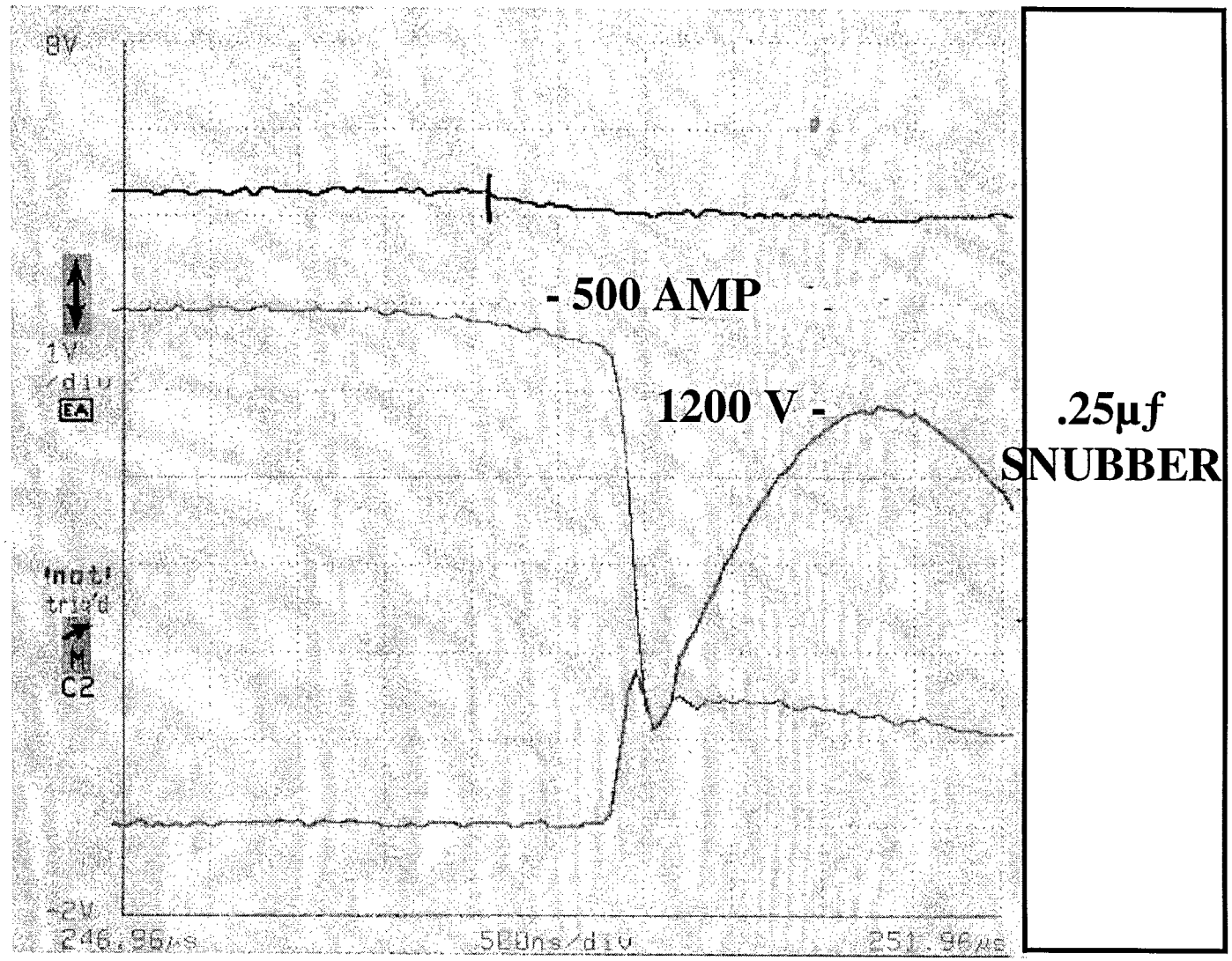

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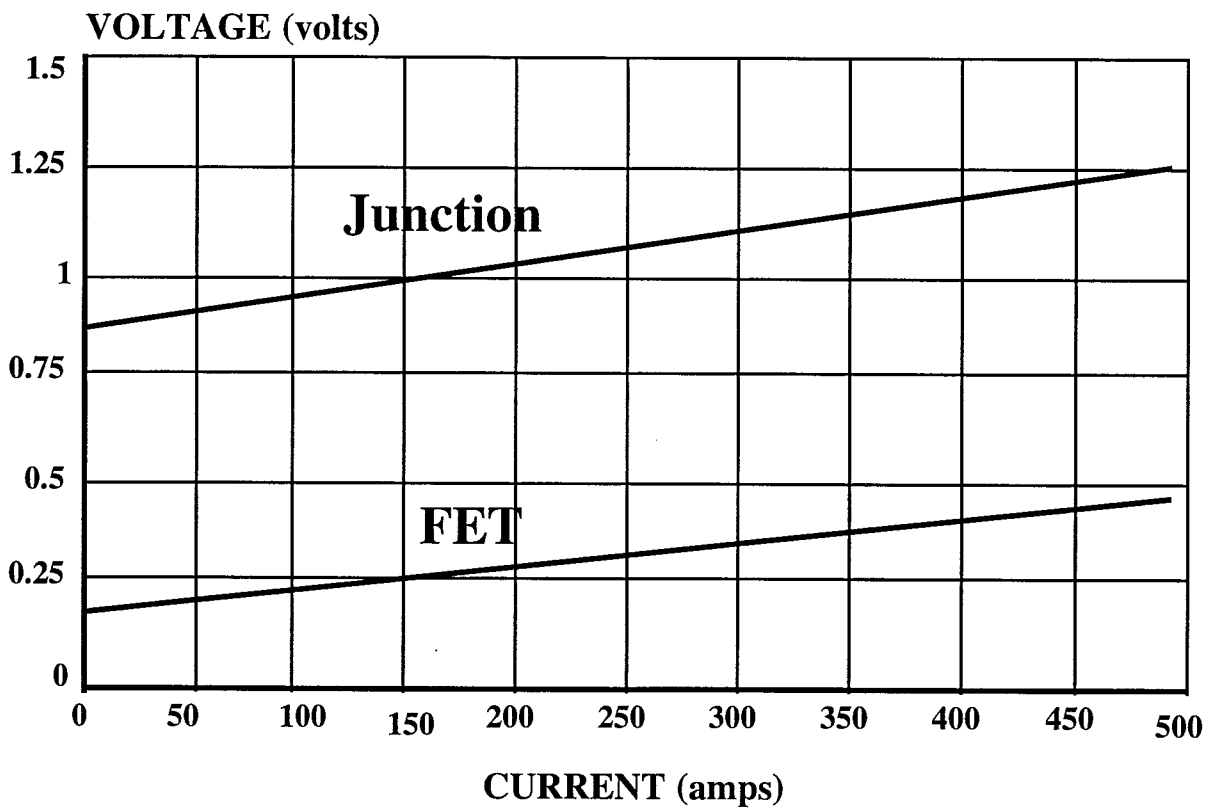
MTO™ Junction & FET Drop

ISO 9001 Certified



Measurement For Determining Transfer Ratio

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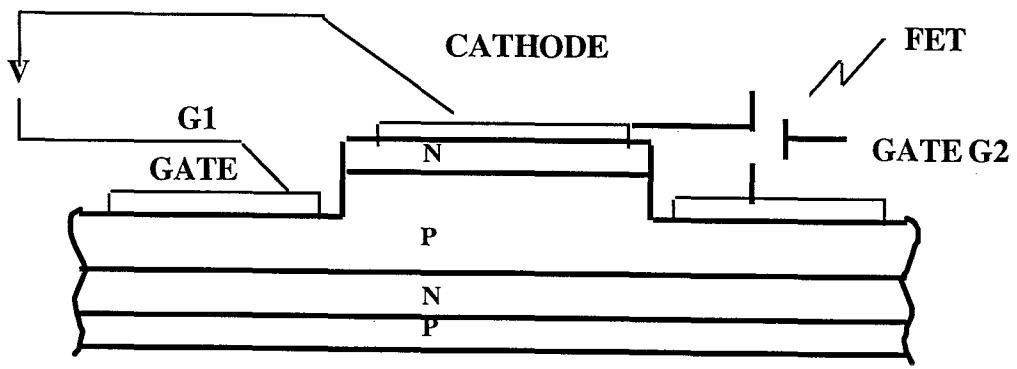
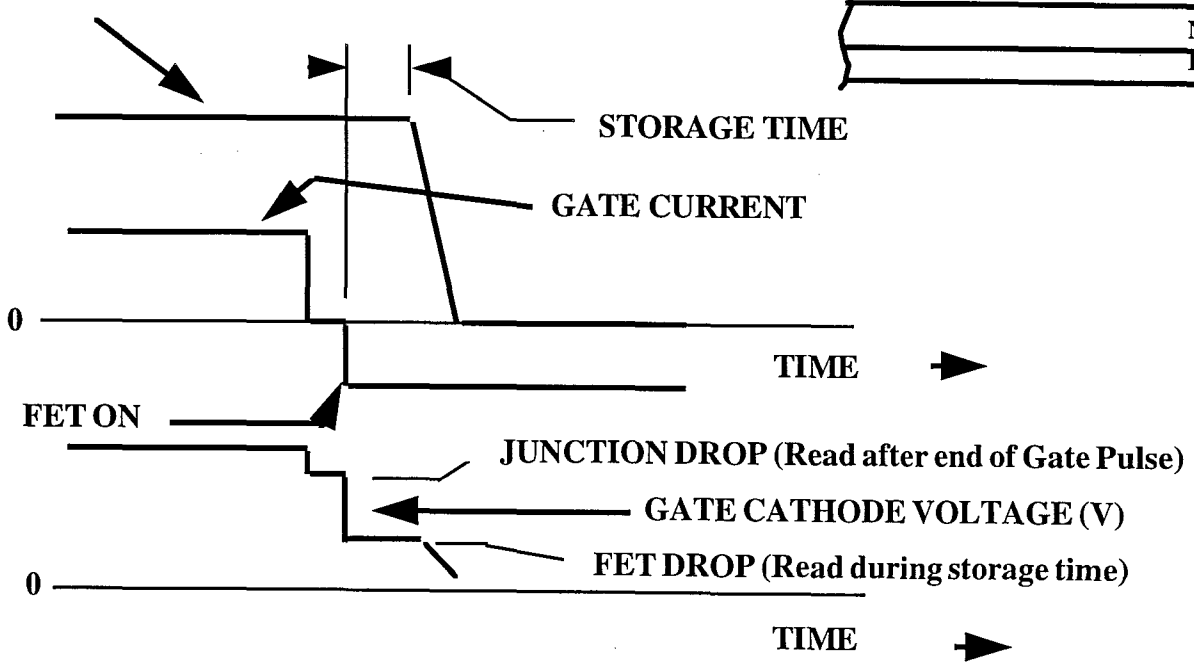
ISO 9001 Certified





G-1 and cathode are used as probes to determine Voltage across emitter junction Vs. voltage across FET, when FET is turned on.

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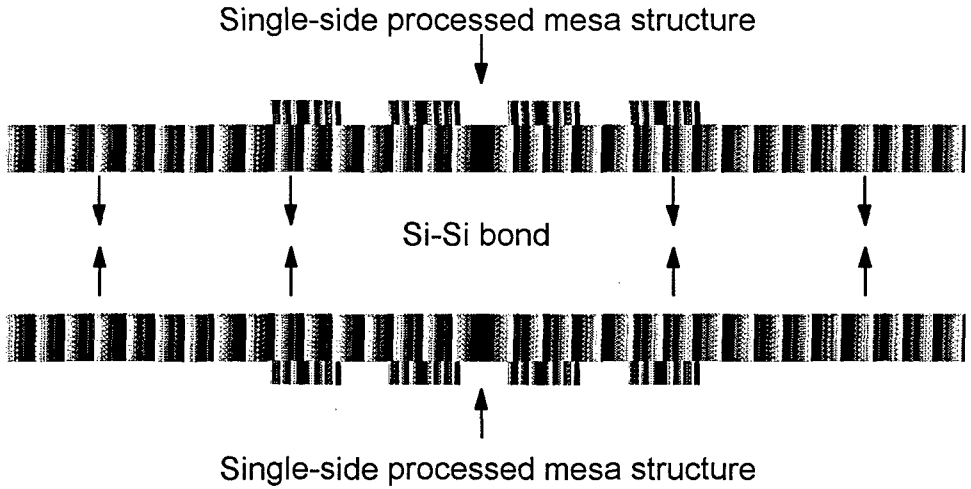
Double side gated MTO™ thyristor



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ADVANCED MTO™ THYRISTOR

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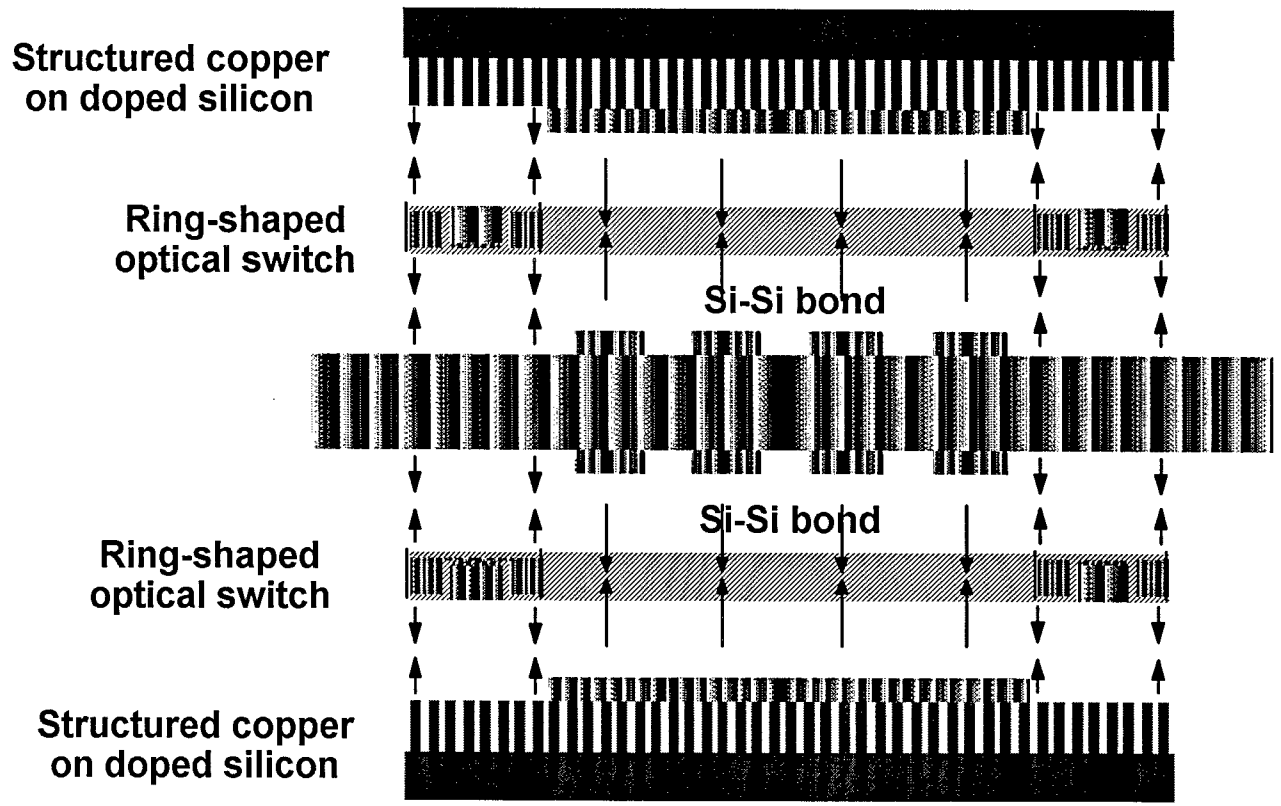
Double side gated MTO™ thyristor with additional silicon bond



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ADVANCED MTO™ THYRISTOR

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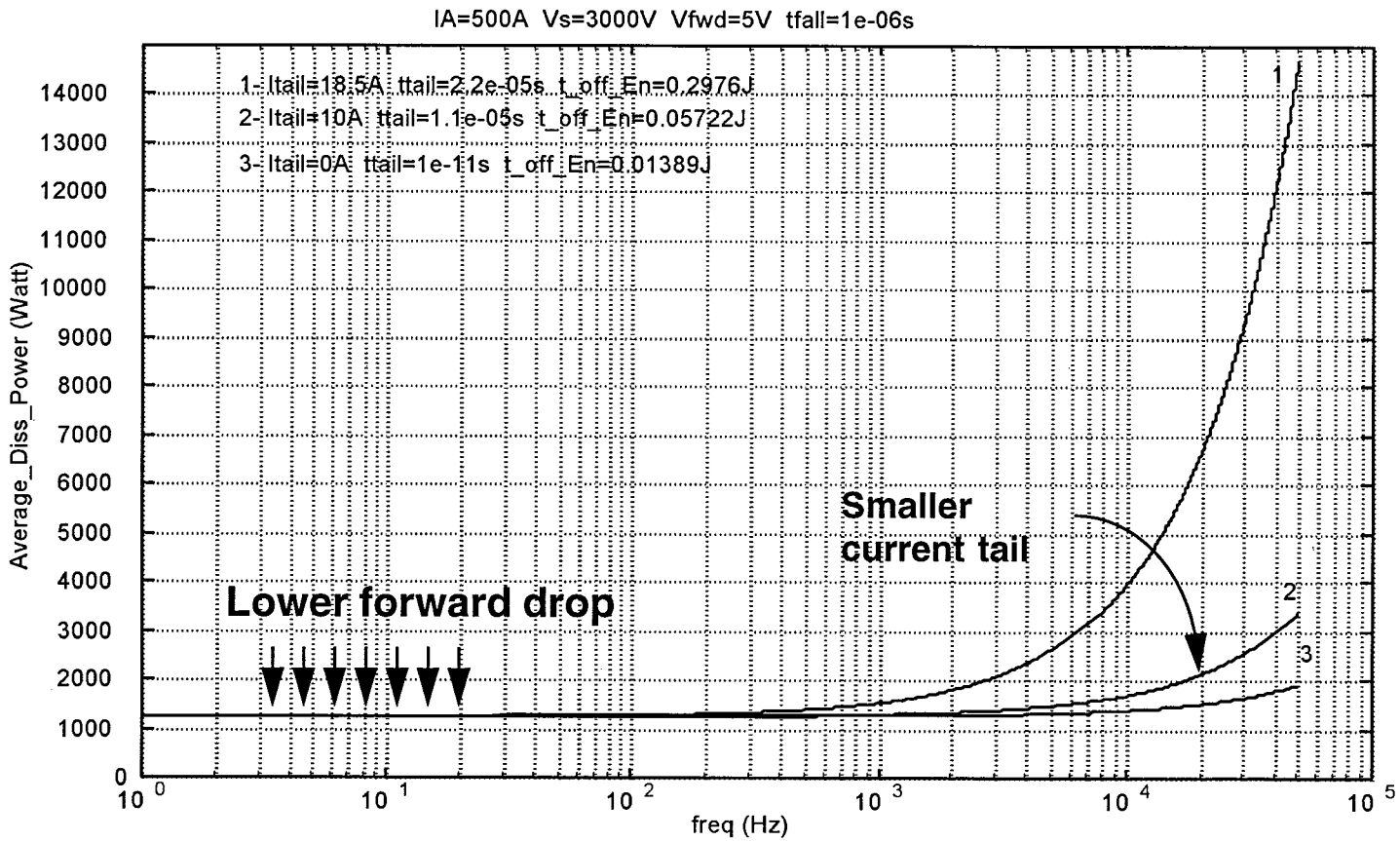
Lower Power Dissipation Expected in Double-Sided MTO Thyristor



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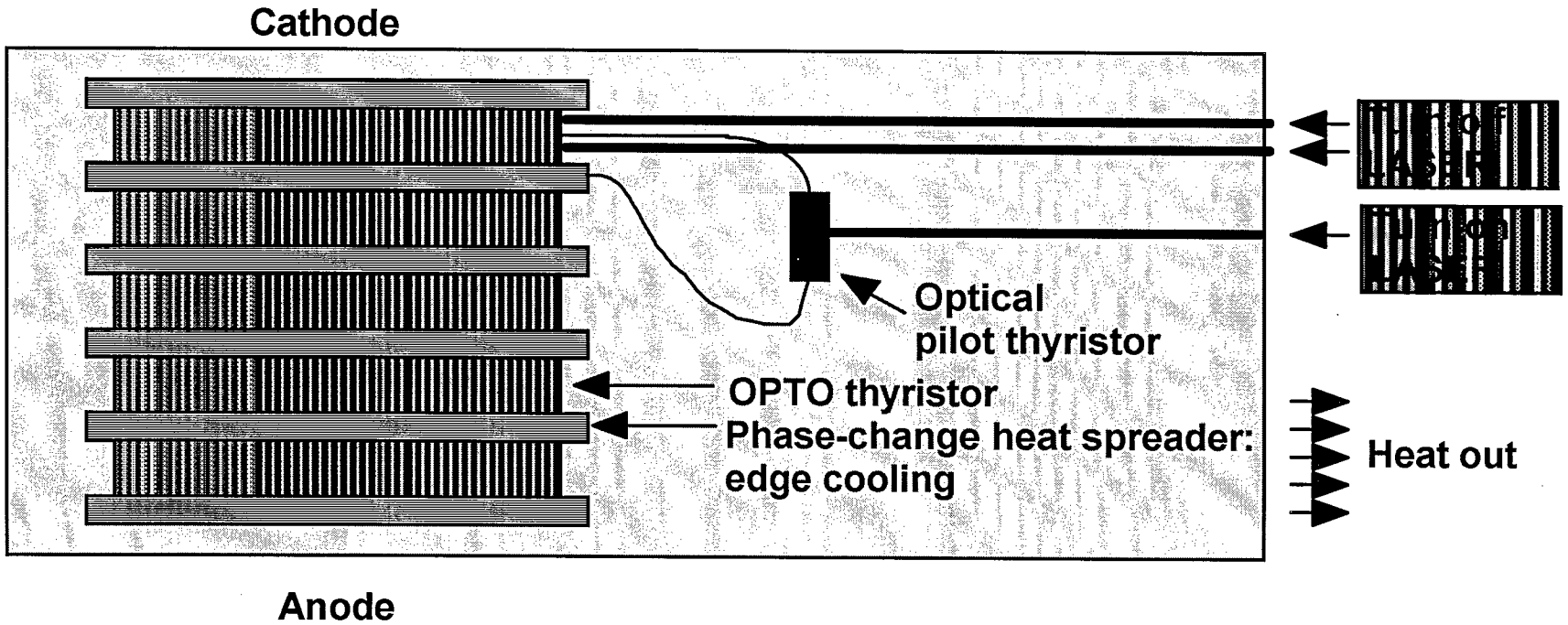
ADVANCED MTO™ THYRISTOR MODULE

ISO 9001 Certified

25kV, 2kA, 10kHz, optically actuated, thermally-managed power module



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Advancements to be made in :

- optical switching
  - ❊ light activated switch in place of FET
- double-sided (low tail)
- low temperature silicon-to-silicon bonding
- phase-change thermal management

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Power Semiconductor Evolution

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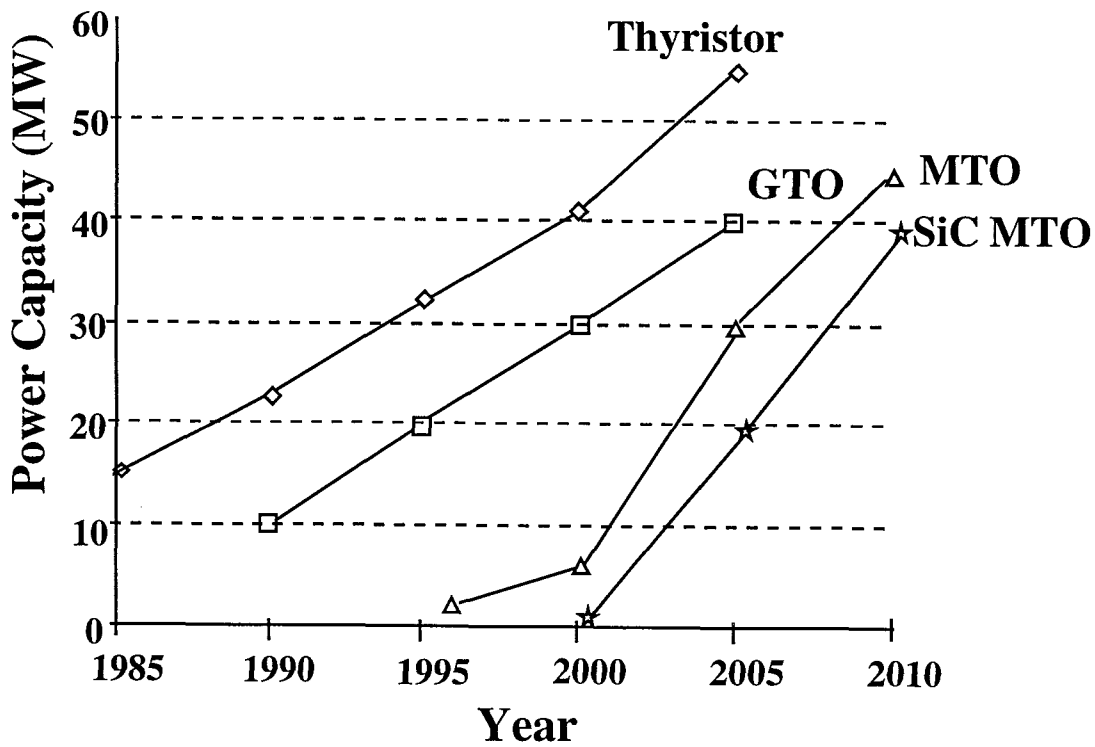
- Higher Voltage Capability
- Faster Switching
- Lower Losses
- Higher Operating Temperatures



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Power Semiconductor Evolution

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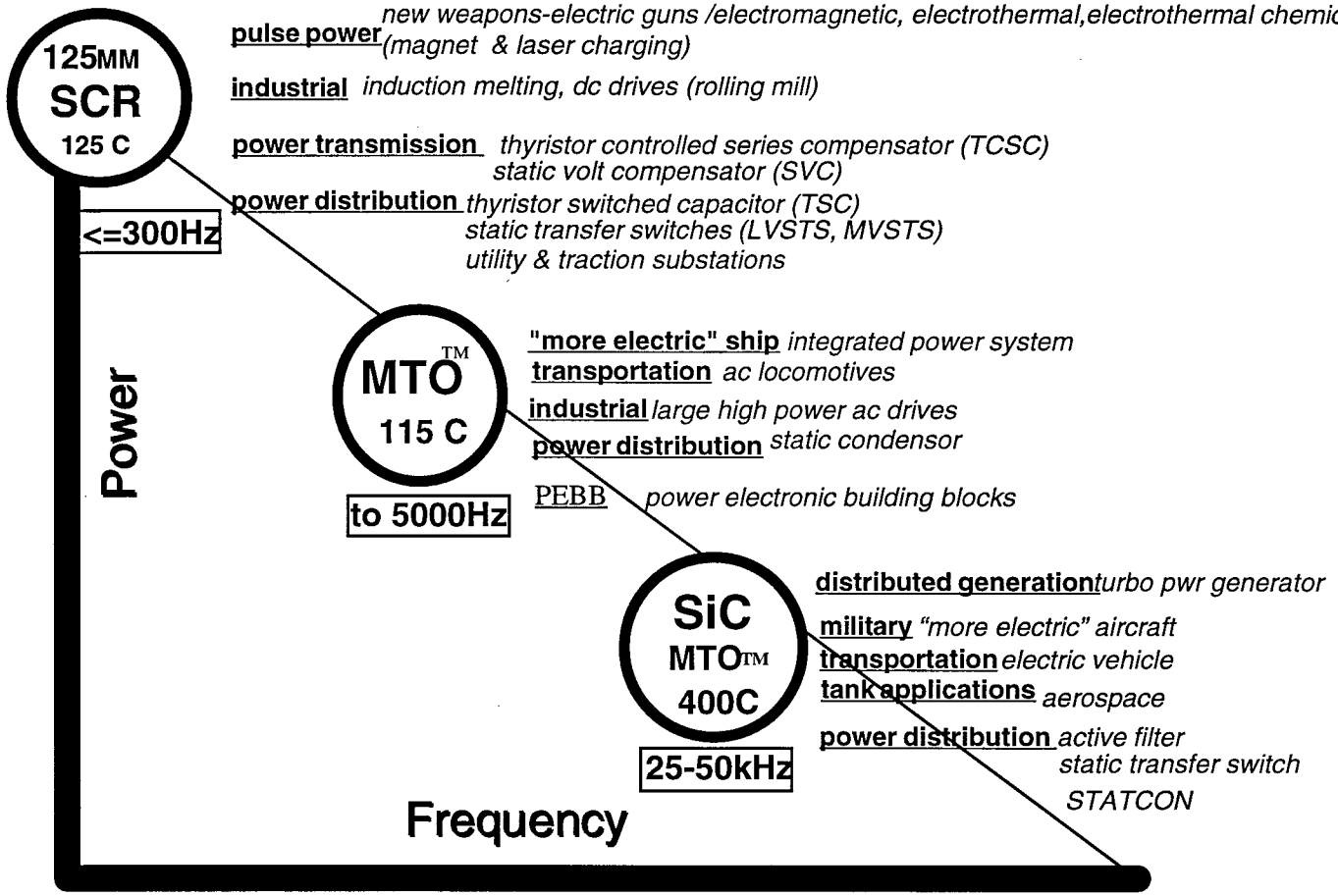

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Packaging of Power Devices - Problems

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Current Technology

- Silicon power devices is pressed between copper posts with strain buffers (tungsten or molybdenum) in between.
- Use of high clamp forces to attain good thermal and electrical contact.
- Relatively high thermal resistance between the dry interfaces and thermal fatigue.
- Use of larger devices magnifies the problem

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Structured Copper - Concept & Benefits

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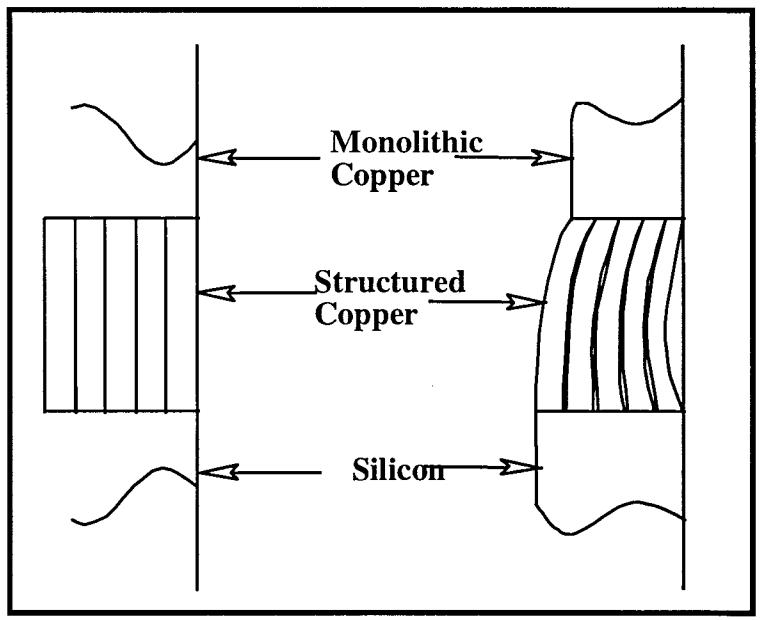
Benefits:

- Higher supression rated devices
- Lightweight assemblies due to elimination of clamps
- Eliminates dry interfaces - lower thermal resistance
- High fatigue rating due to elimination of friction / rubbing



Structured Copper Concept

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Structured Copper bonded to Silicon wafers

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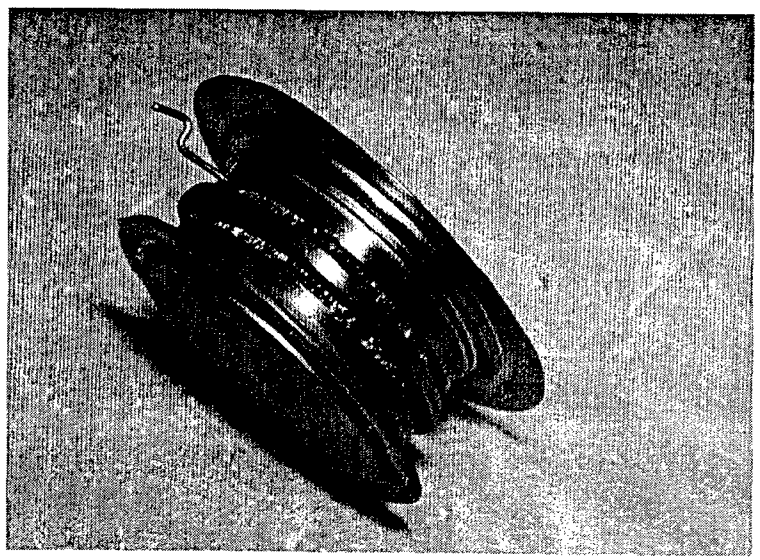

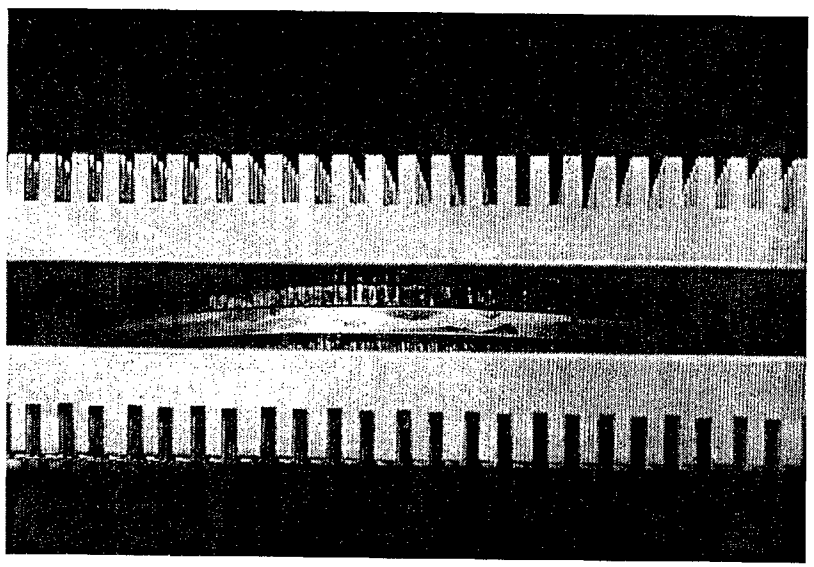

Direct braze / solder bonding to the devices to reduce thermal resistance

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Structured Copper - Performance Benefits

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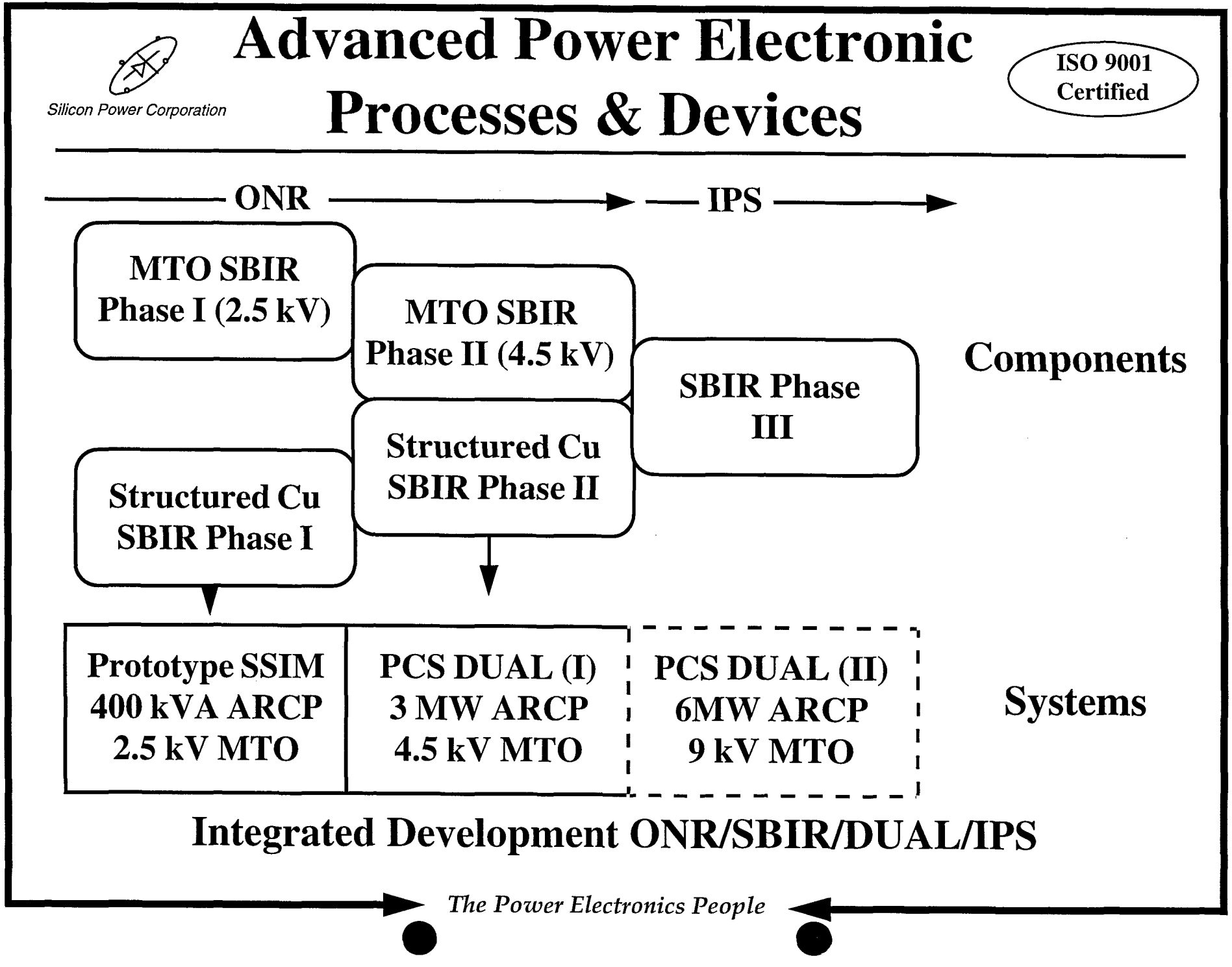
	Standard Press Pak	Str. Copper	% Benefit
Air Cooled	0.05 C/W	0.042 C/W	16
Water Cooled	0.035 C/W	0.027 C/W	23
Submerged Cooled	0.019 C/W	0.011 C/W	42

- **Junction to Coolant thermal resistance becomes more critical with improvement in cooling systems**
- **Improvements in the device surge ratings**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Advanced Power Electronic Processes & Devices
ISO 9001 Certified
ONR
IPS
MTO SBIR Phase I (2.5 kV)
MTO SBIR Phase II (4.5 kV)
SBIR Phase III
Components
Structured Cu SBIR Phase I
Structured Cu SBIR Phase II
Prototype SSIM 400 kVA ARCP 2.5 kV MTO
PCS DUAL (I) 3 MW ARCP 4.5 kV MTO
PCS DUAL (II) 6MW ARCP 9 kV MTO
Systems
Integrated Development ONR/SBIR/DUAL/IPS
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Macro-Processor Module

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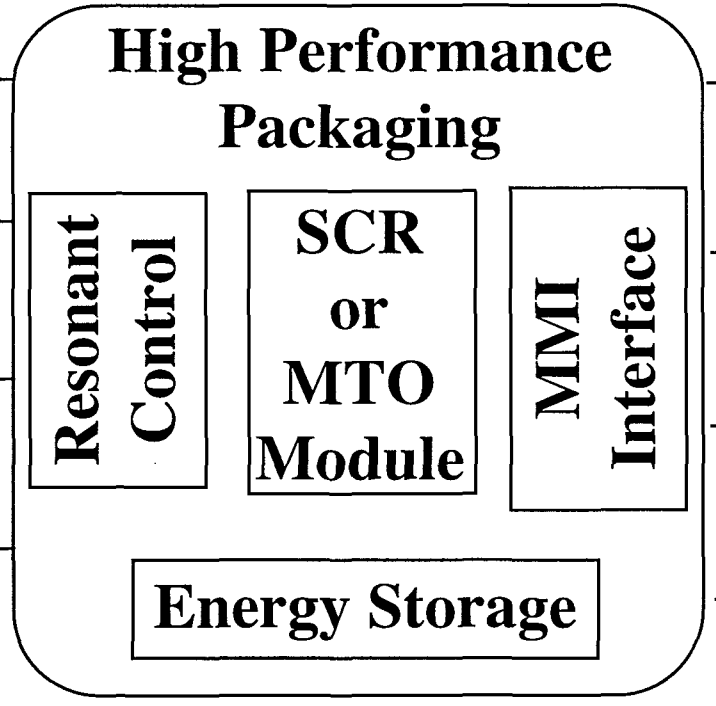
Applications

- Voltage Sags / Outages
- Voltage Regulation
- Transients/ Harmonics
- Propulsion Systems



Products

- STATCON/ UPS
- Static Voltage Regulator
- Active Filter
- PCS

- Power Processor Block
- Flexible Dynamic Performance
- Multiple Functionality

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High Power Electronic Building Block (HPEBB)

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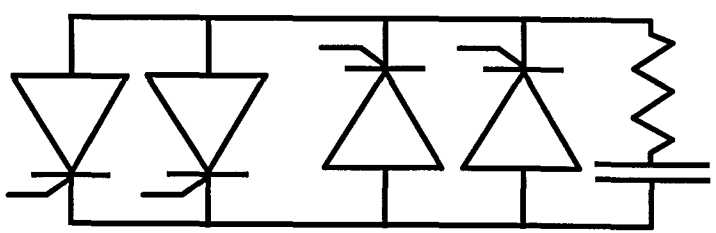
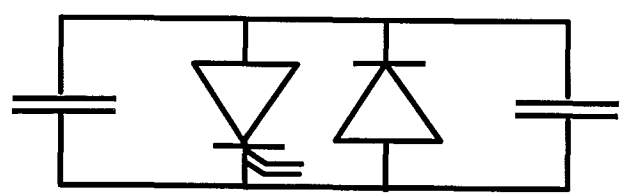
Duality

AC switch



- SCR
- zero current switching
- symmetric blocking
- ride-through capability

Inverter Switch



- MTO™ thyristor
- zero voltage switching
- asymmetric blocking
- interrupting capability

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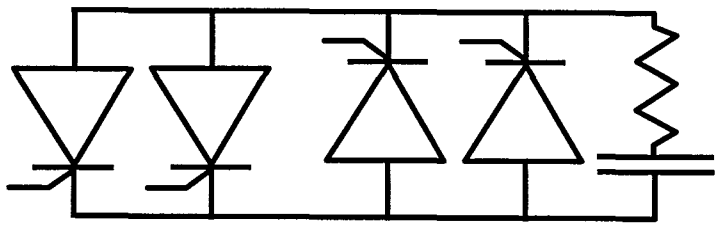
HPEBB - AC Switch

ISO 9001 Certified

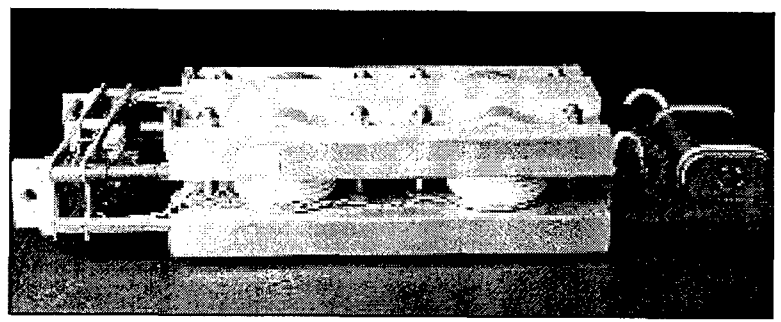


RATINGS

- 480V - 38kV
- 300 - 5000A
- up to 100kA ride-through capability

APPLICATIONS

- Static Transfer Switch
- Static Voltage Regulator
- Static Phase Shifter
- Solid State Breaker
- Fault Current Limiter



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HPEBB - Inverter Switch

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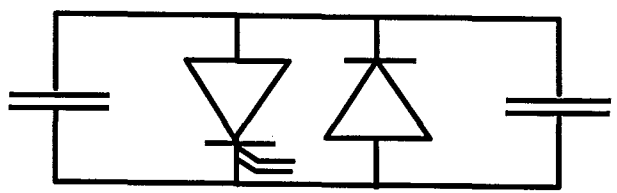
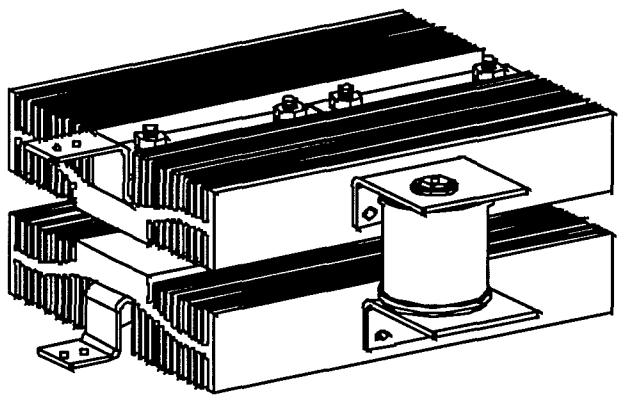


RATINGS

- 0.5 - 6 MVA Inverter
- 480 - 4.16 kVac
- 1.0 - 4.0 kHz

APPLICATIONS

- STATCON/UPS Inverter
- Propulsion Motor Module
- Active filter
- Dynamic Voltage Restorer (DVR)



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PEBB Demonstration Converter

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Reconfigurable Converter System

- Motor Drive (Rect./Inverter)
- Frequency Changer
- Inverter
  - 3-Phase
  - Single Phase H-Bridge
- Rectifier
- DC/DC Converter

Demonstration of ARCP Inverter & MCT as Switching Device

- 50kVA, 750Vdc/450Vac
- $f_s > 20kHz$

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PEBB Demonstration Converter

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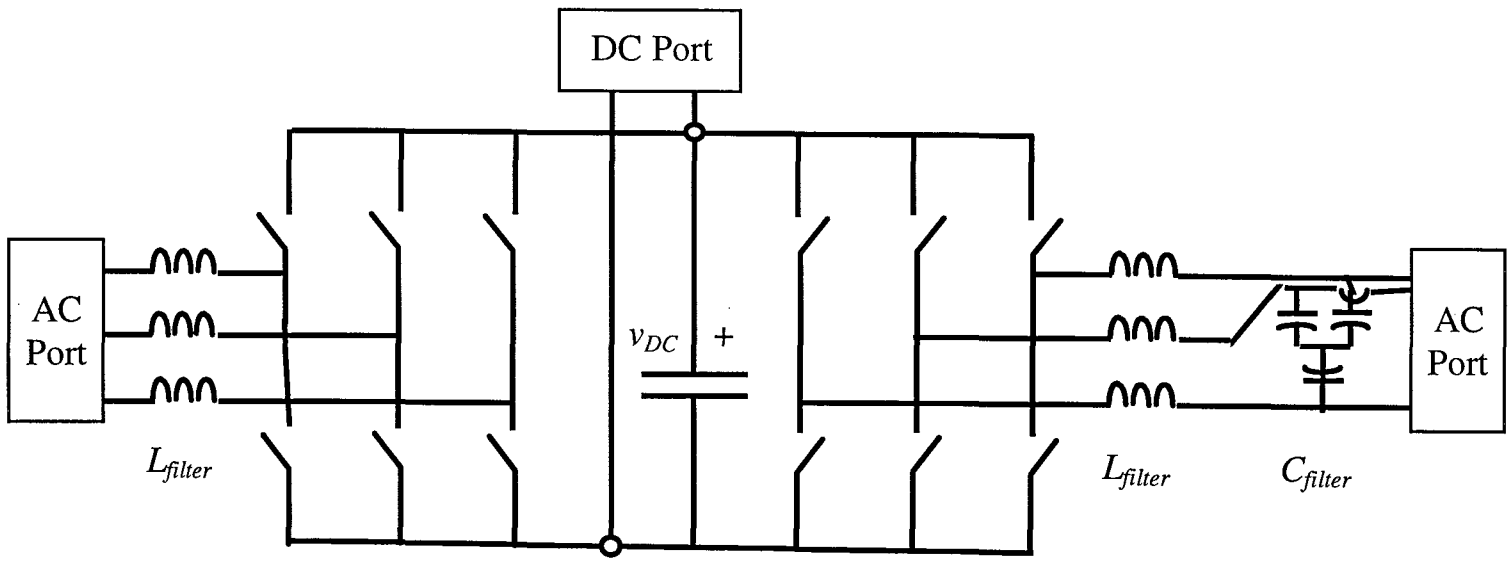
Power Circuit



The six phase-leg converter power circuit (excludes protective / pre-charging and reconfiguration circuits).

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PEBB Demonstration Converter

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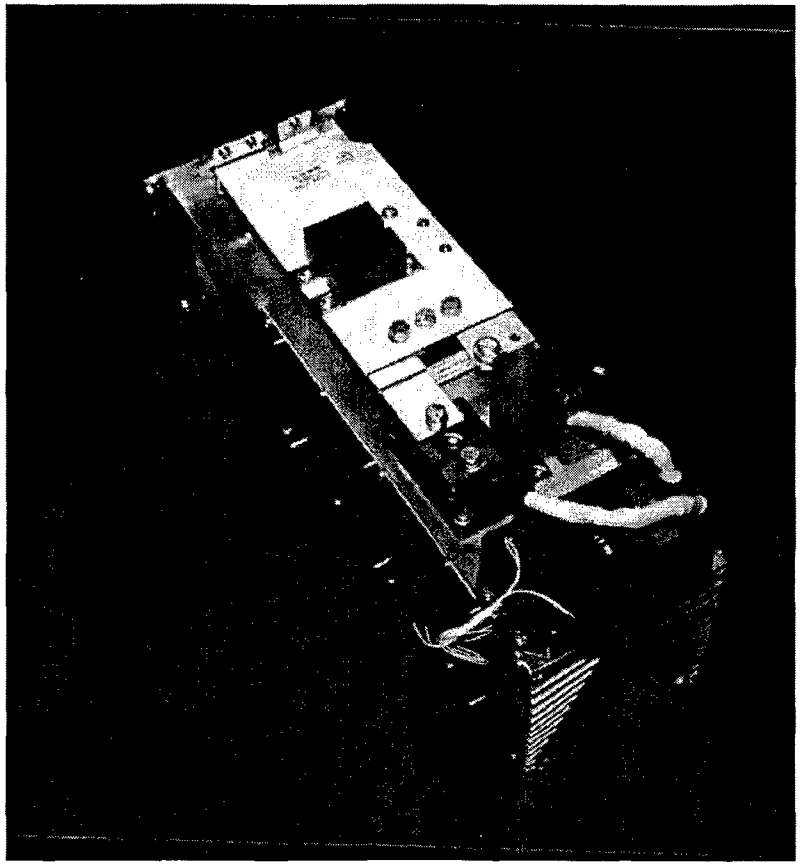
Phase Leg Module



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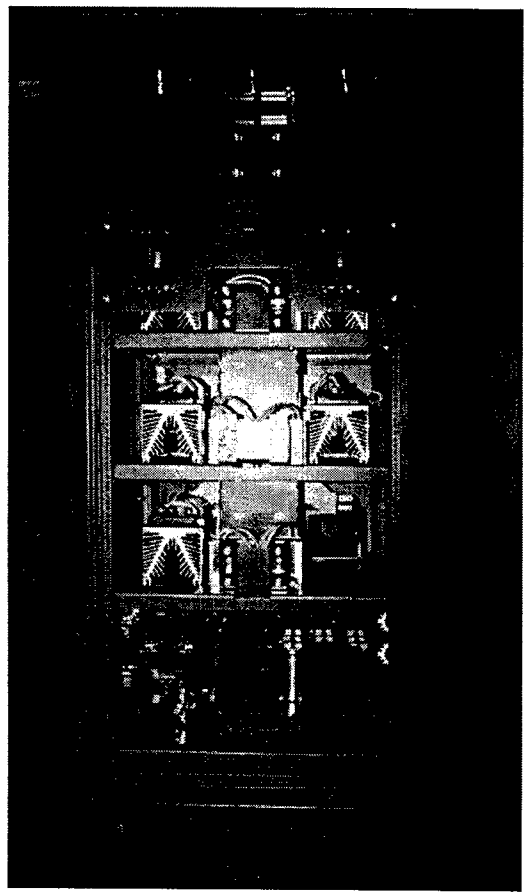
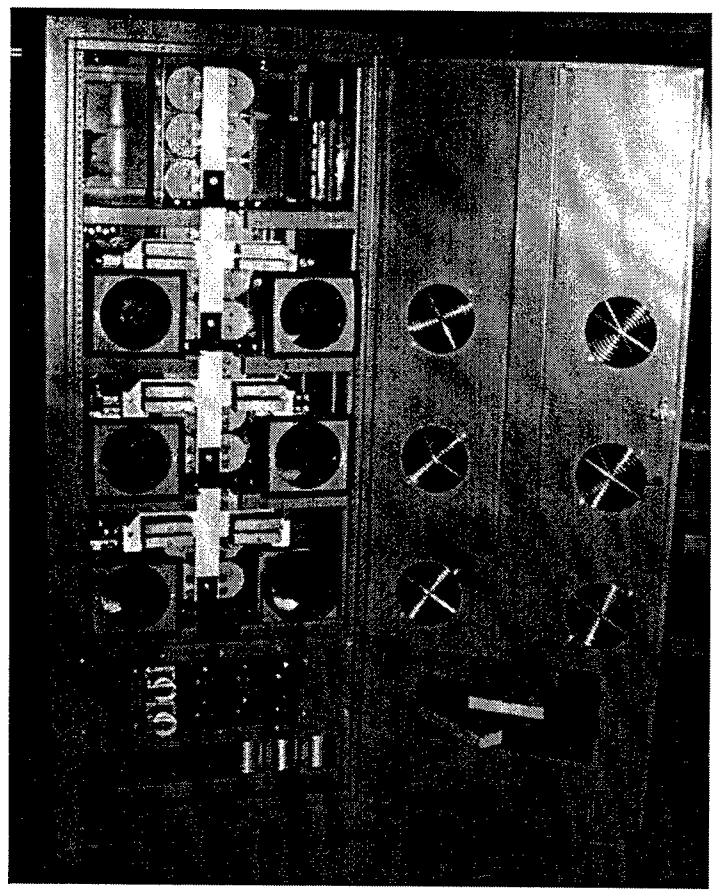
PEBB Demonstration Converter

ISO 9001 Certified





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Ship Service Inverter Module
SSIM

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Certified

Demonstration of MTO Thyristors in ARCP Circuit

400kVA, 3-Phase ARCP Inverter

- MTO Thyristors used as switching devices (main & auxiliary)
- 0-60 Hz operation
- 1,500 Vdc bus
- 1,150 Vac output

-

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Ship Service Inverter Module
SSIM

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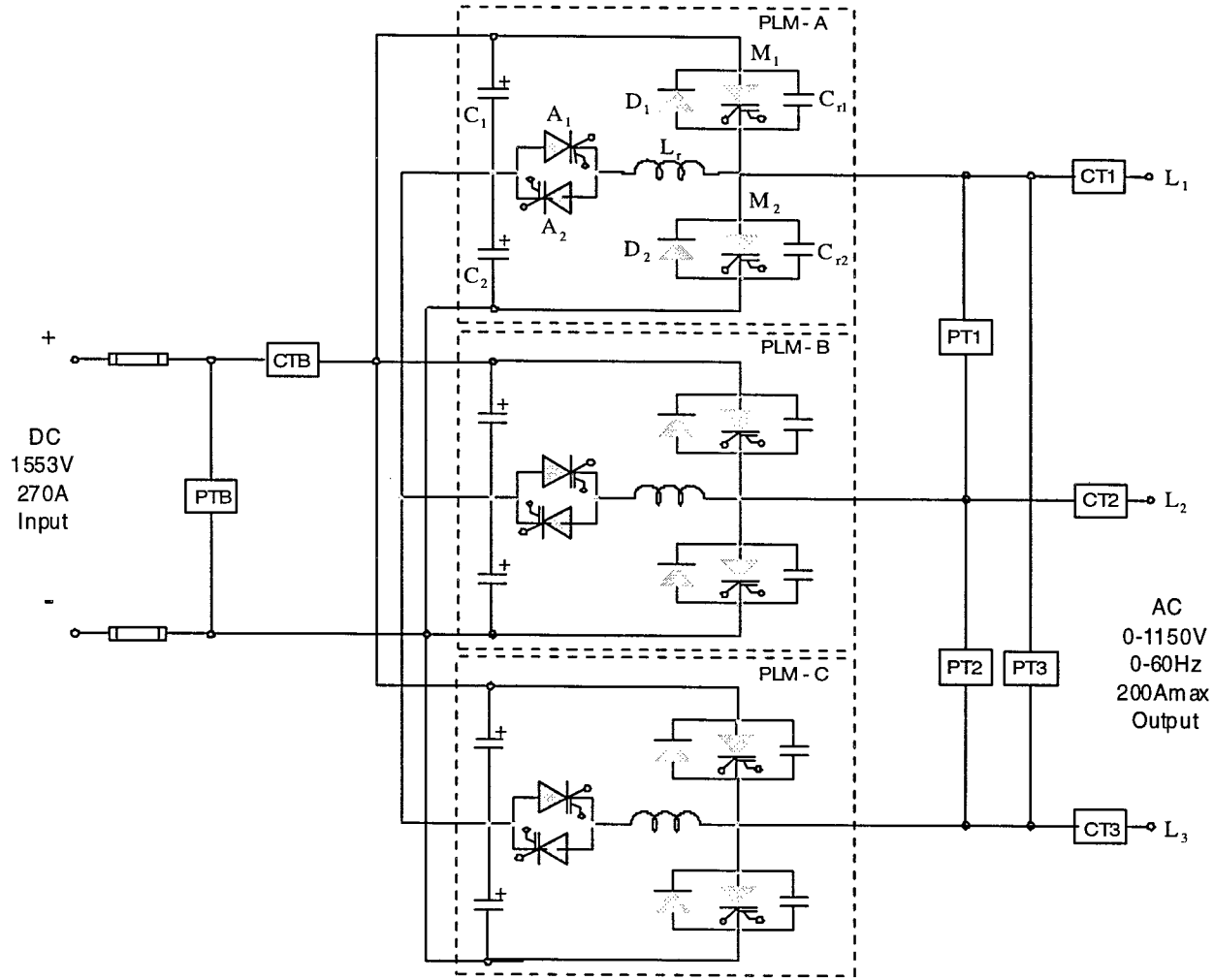

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Power Conversion System
PCS

ISO 9001
Certified

3.3 MVA, 3-Phase ARCP Inverter w/ Energy Storage

- MTO Thyristors used as switching devices (main & auxiliary)
- 60Hz operation
- 3.3 kVdc bus
- 2.4 kVac output
-

Dual use program with ONR

- Military Use - Propulsion Drives, DC/DC Converters
- Commercial Use - STATCON/UPS

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R&D -> Product Manage Risks / Rewards

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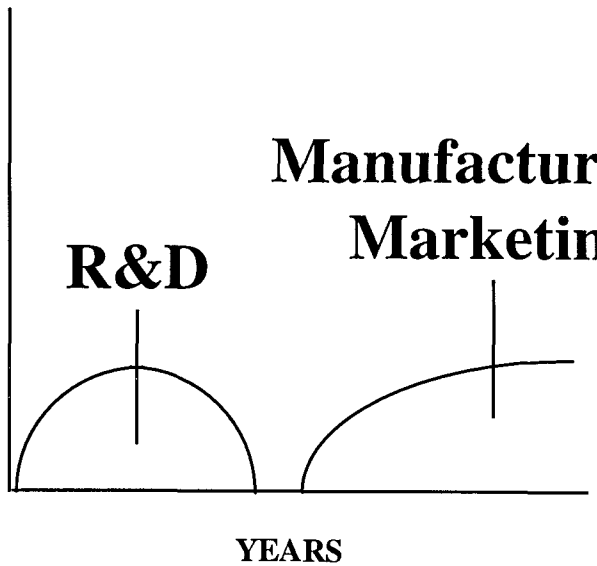
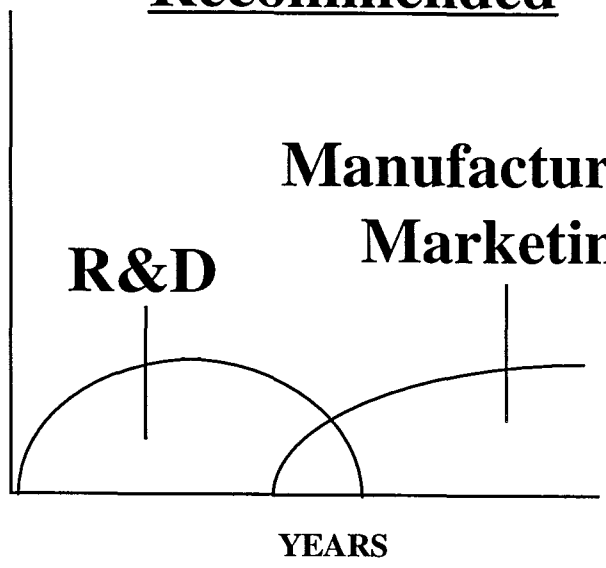
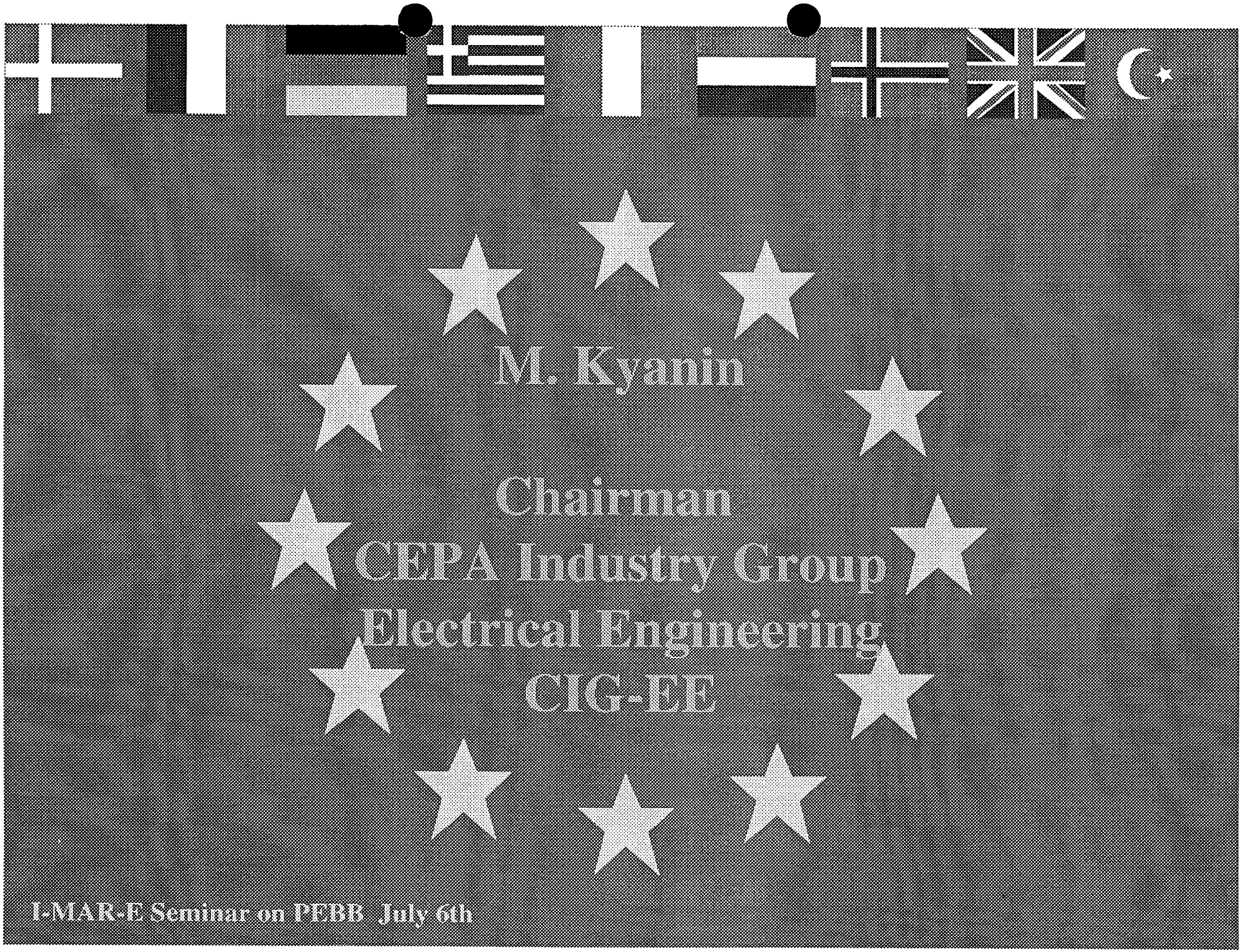


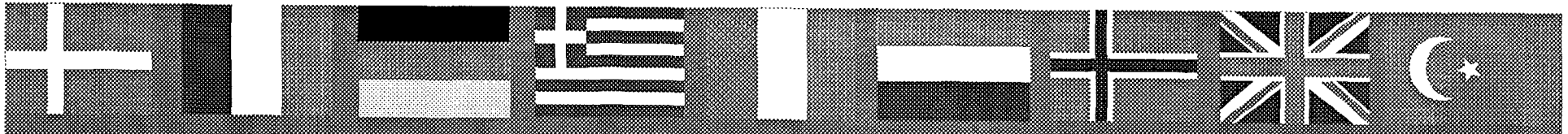
- Low risk - manufacturing
- Lack of user feedback
- Commercialization at high risk

Recommended



- Optimum product strategy
- Fuels continuous improvement and next generation technology/ products
- Moderate risks - can be minimized by proper planning


M. Kyanin
Chairman
CEPA Industry Group
Electrical Engineering
CIG-EE
I-MAR-E Seminar on PEBB July 6th



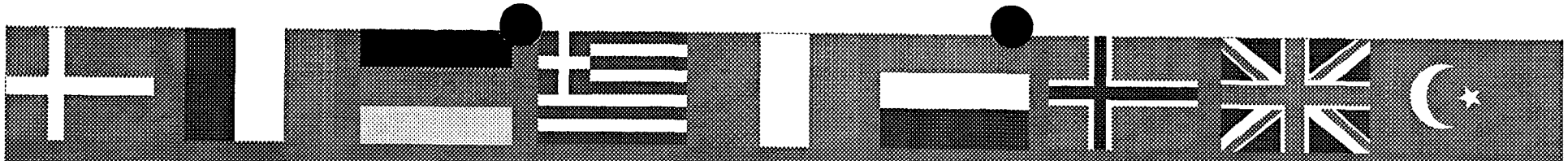
Mischa Kyanin

IMTECH Marine & Industry / R&H Systems

Manager (Netherlands) Defence activities

phone +31 10 487 1606 fax +31 10 487 1745

Chairman of CIG-EE



EUCLID

European Coorporation for the Long term In Defence

- Initiative of the R&T group (panel II) of the Western European Armaments Group (WEAG)

The Purpose

- The purpose of EUCLID is to strengthen the European position regarding Defence Research & Technology

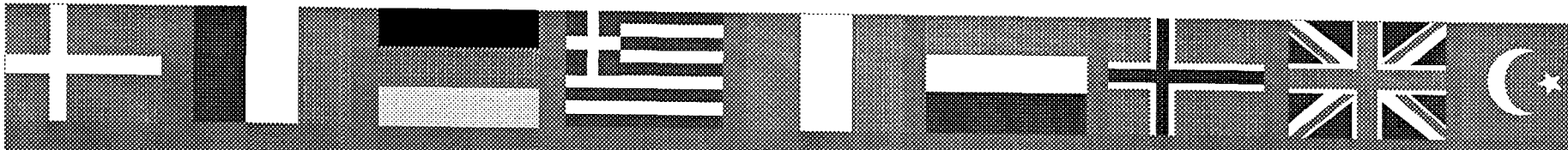
Performed by:

- both Industries and Institutes participate in EUCLID projects

Principle:

- Each participating country finances its own R&T, no border crossing of money

The total amount of the EUCLID programme is approx 200 M ECO per annum



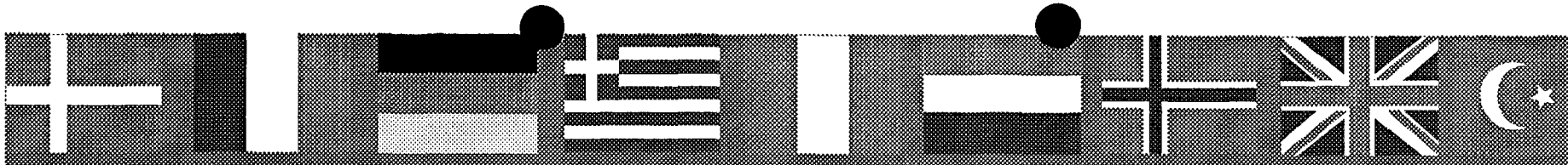
Participating Countries
WEAG

Ireland
Finland
Austria
Sweden

Belgium
Denmark
France
Germany
Greece
Italy
Luxembourg
Netherlands
Portugal
Spain
United Kingdom

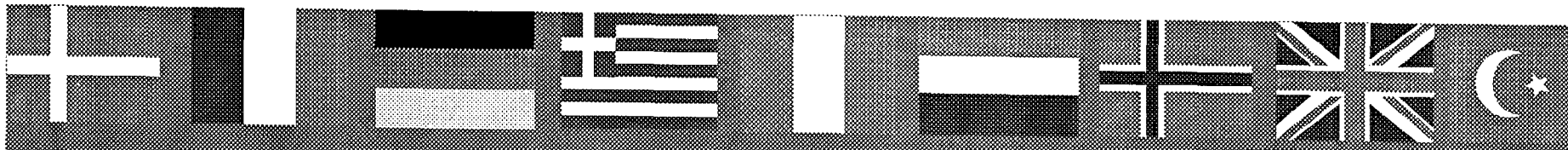
Iceland
Norway
Turkey

USA
Canada



EUCLID Procedures

- EUCLID
  RfQ by Gov'ment, response by Industry and/or Institutes. Funded by Governement and the Industry
- THALES ("Joint Programme", JP)
  Same as EUCLID, only for Institutes
- EUROFINDER
  Proposal by Industry, Contract by Governement



EUROFINDER - Principles

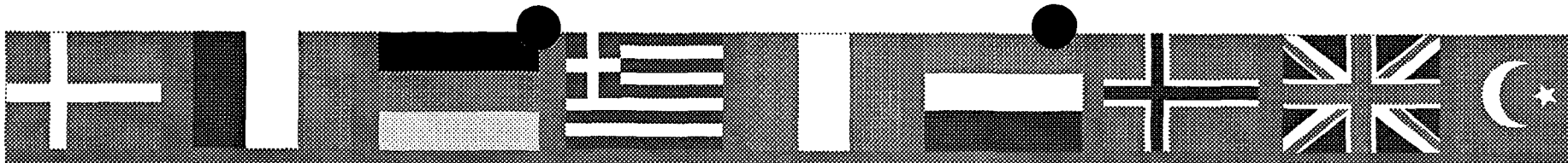
Focus: Proposals are to be offered in existing CEPA's, without conflicting other RTP's.

Participation: Open to all WEAG nations.

Equal shares: Contributions by all governments shall be equal.

Industrial Contribution: The industry contribution shall at least match the government contribution.

Competition: Open announcement of the RfQ in all participating nations, selection of the best / most cost effective.

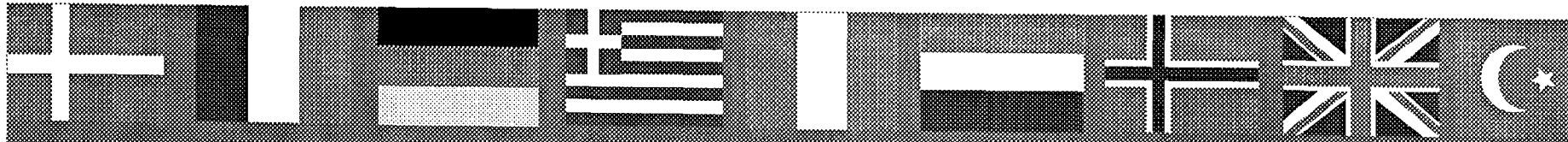


Terms of Reference CEPA-EE

During 1996, PANEL II started a new CEPA in response of ALL ELECTRIC "platform" developments, mainly ships and vehicles.

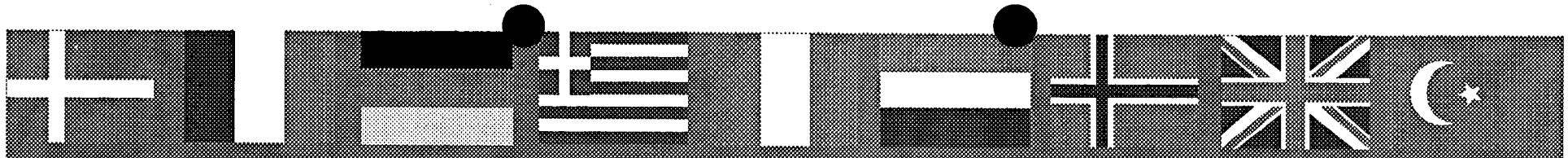
Military needs:

- Improve weight and volume efficiency,
- reduce Life Cycle costs,
- improve reliability and maintainability.



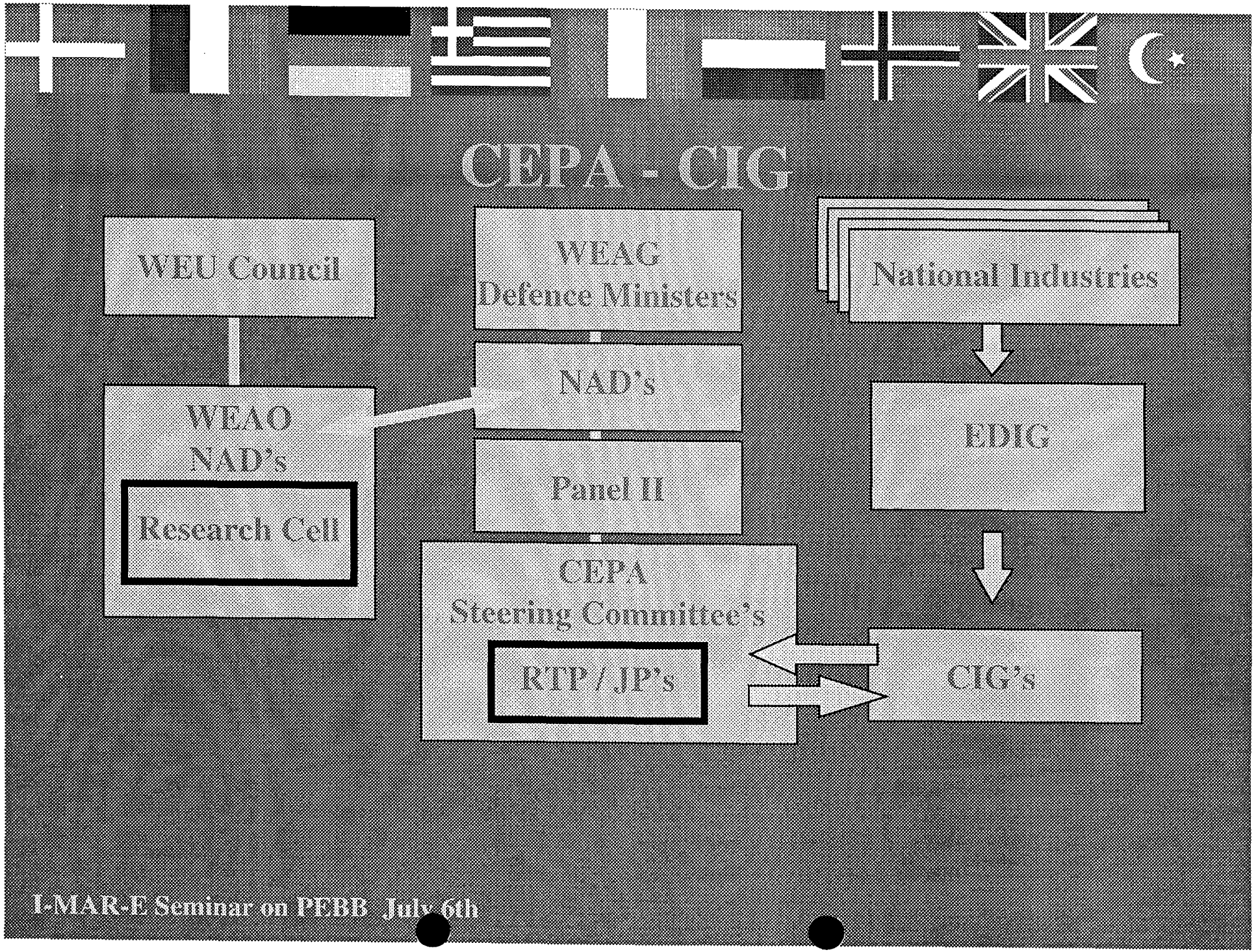
R&T Funding

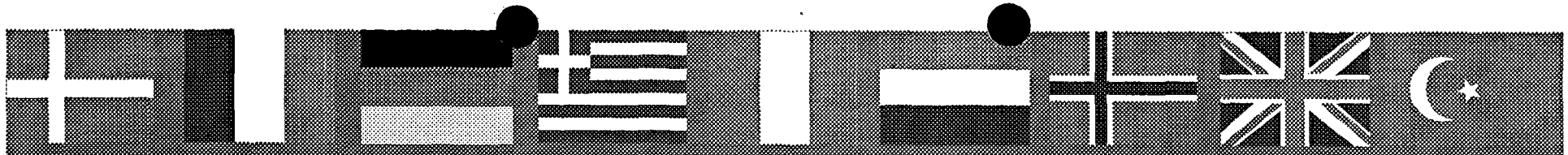
- All R&T funding by WEAG governments:
  - 1995: 2310 MECU
  - 1996: 2270 MECU
  - 1997: 2330 MECU
- CEPA-EE:
  - JP-1: >3 MECU
  - JP-4: > 1 MECU
  - RTP-6:> 6 MECU



Organisation of CEPA's and CIG's

- CEPA 1 Modern radar Technology (GE)
- CEPA 2 Micro - Electronics (FR)
- CEPA 3 Advanced materials and structures (UK)
- CEPA 4 Modular Avionics (GE)
- CEPA 6 Advanced information processing and communication (FR)
- CEPA 8 Opto Electronics (IT)
- CEPA 9 Satellite surveillance technology (NO)
- CEPA 10 Underwater technologies (UK)
- CEPA 11 Defence modelling and simulation technologies (NL)
- CEPA 13 Chemical and biological defence technology
- CEPA 14 Energetic materials (UK)
- CEPA 15 Missile guidance and control technology (FR)
- **CEPA EE (16) Electrical Engineering (NL)**


CEPA - CIG
WEU Council
WEAG
Defence Ministers
National Industries
NAD's
WEAO
NAD's
Research Cell
EDIG
Panel II
CEPA
Steering Committee's
RTP / JP's
CIG's



Project overview

- JP-1 Sea Systems integration

  A series of scoping studies to address both equipment and system requirements for AES

- JP-2 Land Systems integration

  As JP-1, for All Electric Vehicle

- JP-4 Energy Storage

  Combine increased volumetric and mass efficiency, seeking rapid discharge capability and peak/pulse power performance (rotating, superconduct. coils, capacitors, batteries)

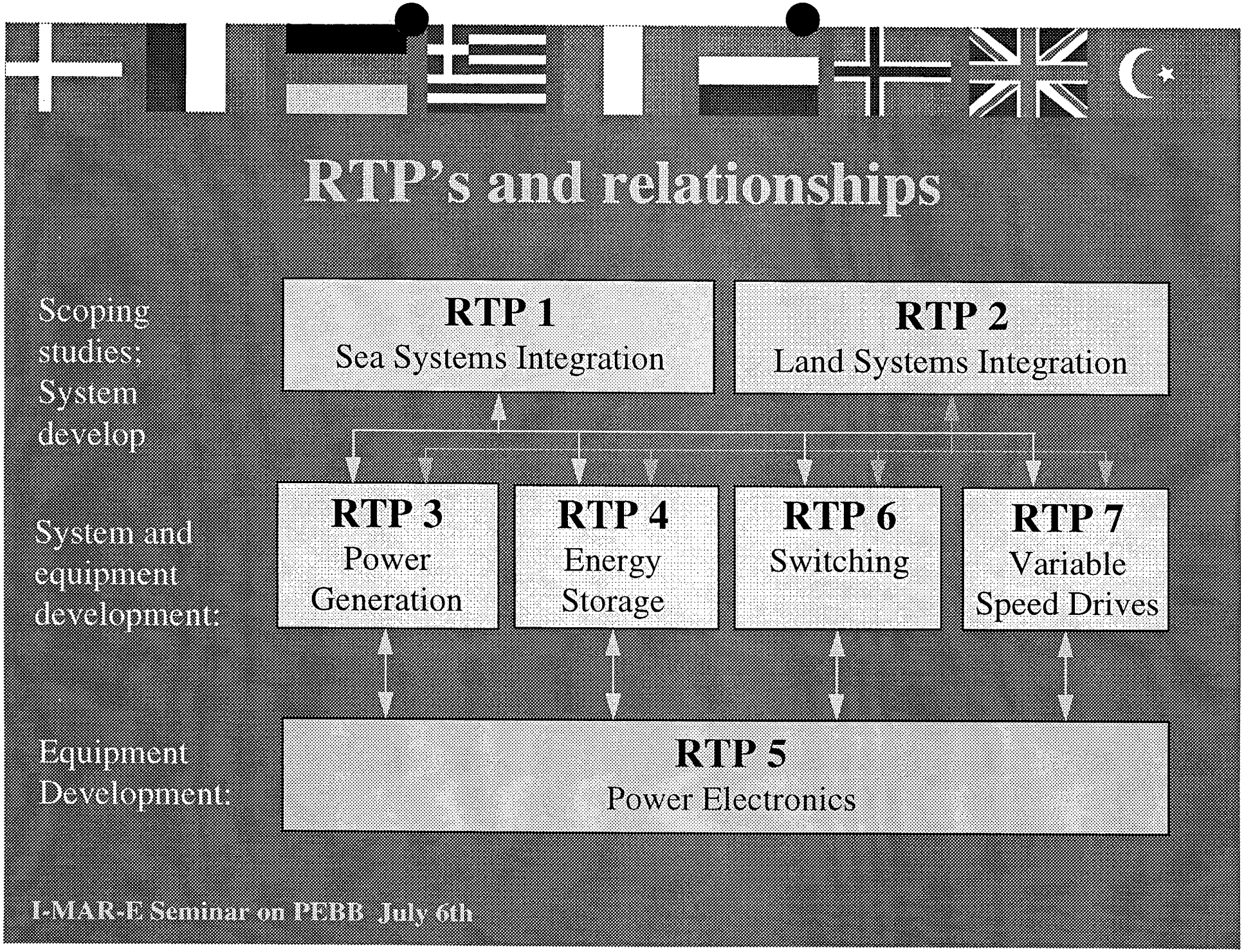
- RTP-6 Switching Technology

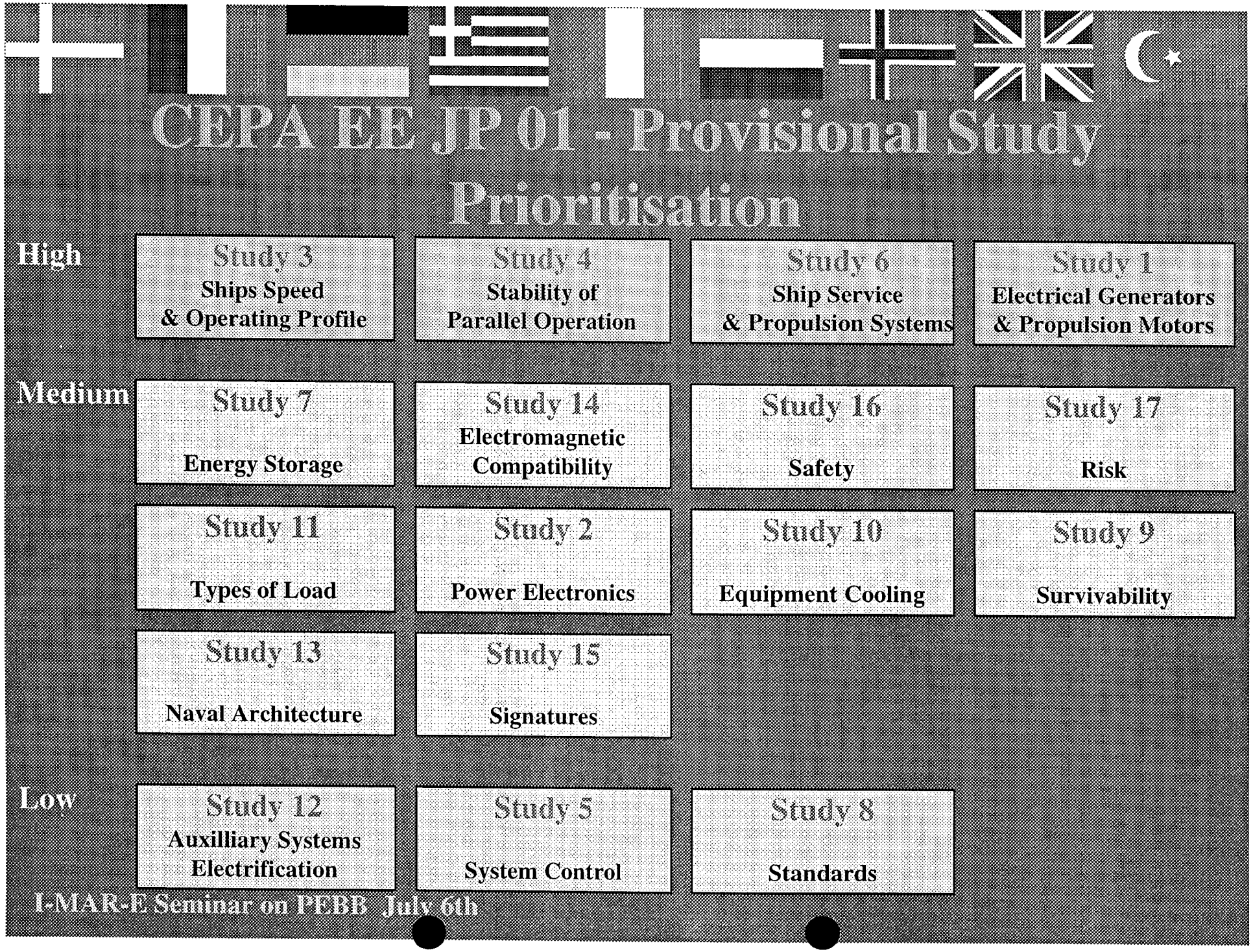
  In networks, focussed on high current / high voltage switching

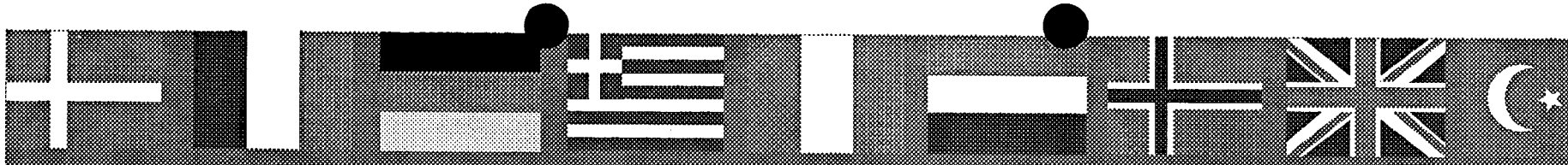
Projects within CEPA-EE

	Steering Committee	JP-1 Sea	JP-4 Energy	RTP-6 Switching	JP/RTP-2 Land Systems
NI					
BE					
DE					
FR					
GE					
GR					
IT					
NO					
TU					
UK					

RTP's and relationships



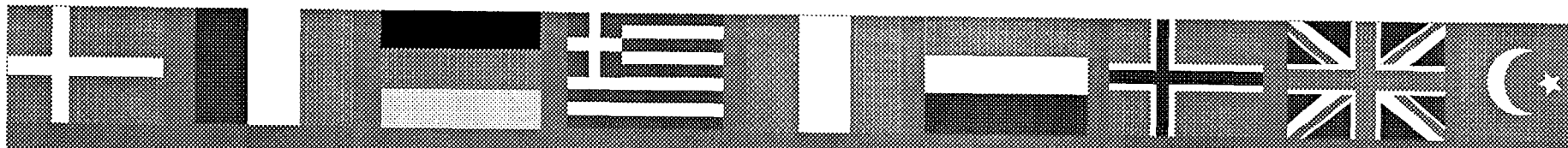

CEPA EE JP 01 - Provisional Study
Prioritisation
High
Study 3
Ships Speed
& Operating Profile
Study 4
Stability of
Parallel Operation
Study 6
Ship Service
& Propulsion Systems
Study 1
Electrical Generators
& Propulsion Motors
Medium
Study 7
Energy Storage
Study 14
Electromagnetic
Compatibility
Study 16
Safety
Study 17
Risk
Study 11
Types of Load
Study 2
Power Electronics
Study 10
Equipment Cooling
Study 9
Survivability
Study 13
Naval Architecture
Study 15
Signatures
Low
Study 12
Auxilliary Systems
Electrification
Study 5
System Control
Study 8
Standards
I-MAR-E Seminar on PEBB July 6th



Preliminary conclusion

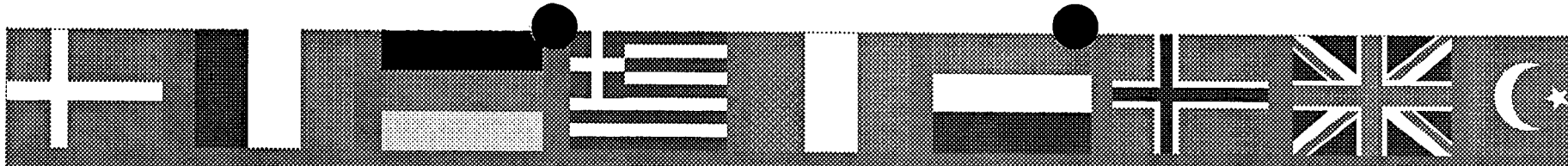
PEBB relates to:

- RTP-5 / Power Electronics
- JP-1



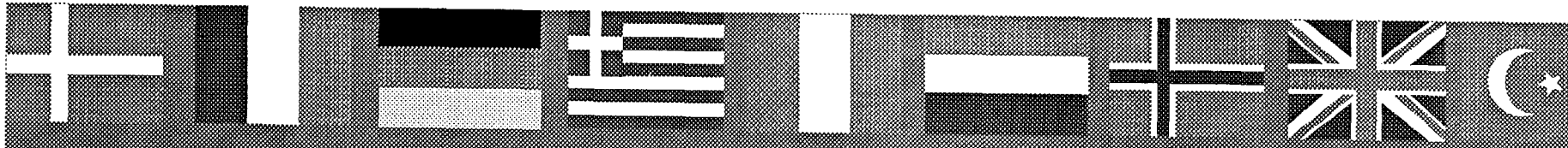
CIG - EE Members

Belgium	Seeking
Denmark	Seeking
France	Yes, incl. Thomson, Alstohm, GIAT etc.
Germany	Yes, incl. DASA, MaK etc.
Greece	Seeking
Italy	Yes, incl. Alenia, Ansaldo etc.
Luxembourg	Seeking
Netherlands	Yes, incl. Fokker/Stork, ECN etc.
Portugal	Seeking
Spain	Seeking
United Kingdom	Yes, incl. BMT, Cegelec etc.



Identified technology developments

- Power generation
  Fuel efficiency and power density
  1 -- 10 Mwatt. Fuel cells ?
- Power Electronics
  Low Loss / High temperature
- Variable speed drives
  Motor controls, widely programmable, including electromagnetic bearings and suspensions
- Pulse forming
  High power / high voltage



Possible Relationship

- CEPA 2 — semiconductor components
- CEPA 3 — material for construction
- CEPA 4 — power equipment

- EU programmes (f.e. JOULE, THERMIE)

- NATO / NIAG

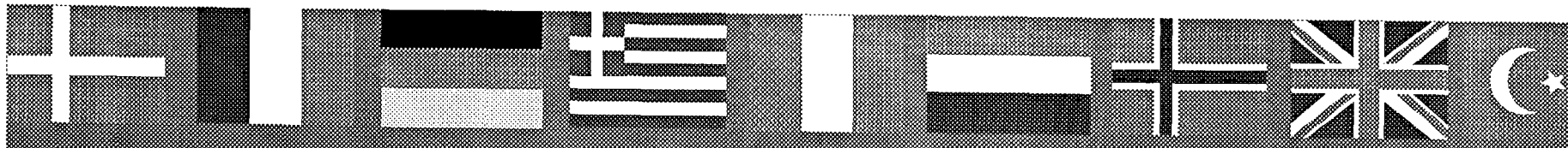
NIAG vs CEPA

- DISCUSSION ON INTELLECTUAL PROPERTY

CEPA EE, JP-1

ALL ELECTRIC SHIP

NIAG study



Related initiatives

- "clean ship" initiative
- fuel cell application
- permanent magnet engines
- high speed (GT) generators
- fuel reforming

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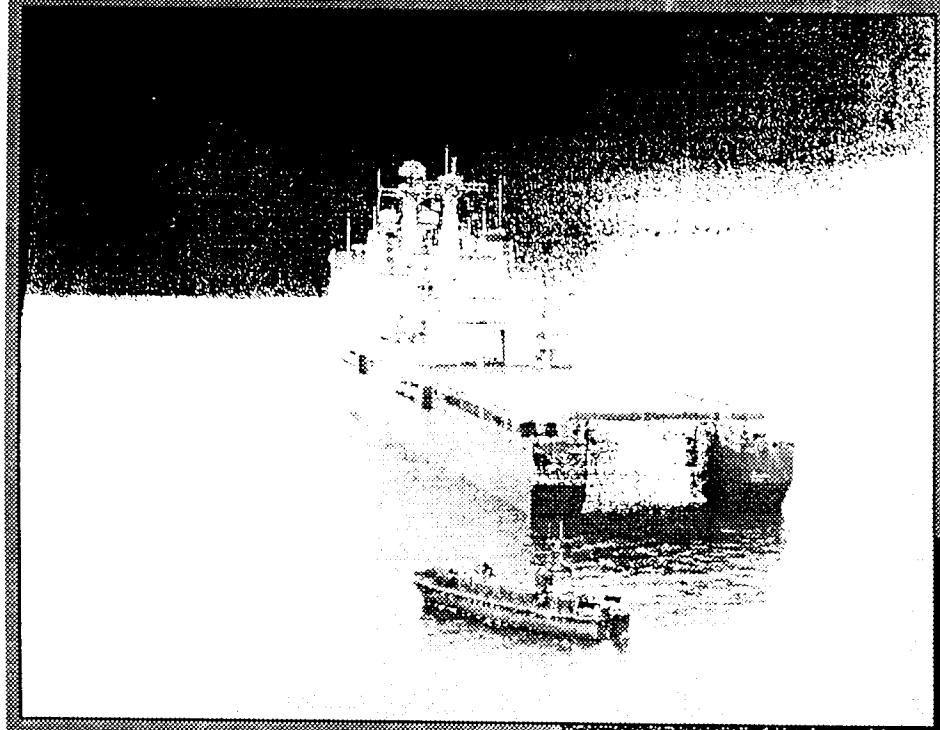
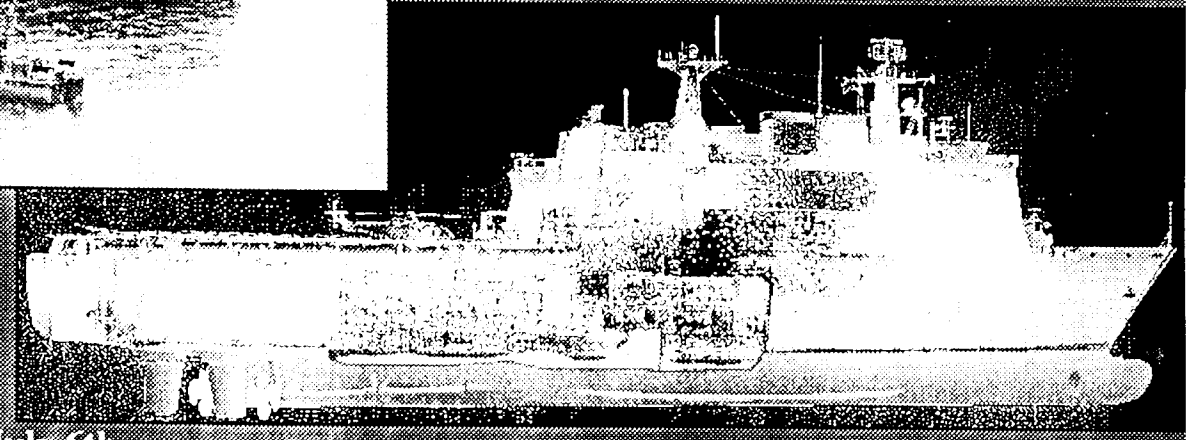
Typical example

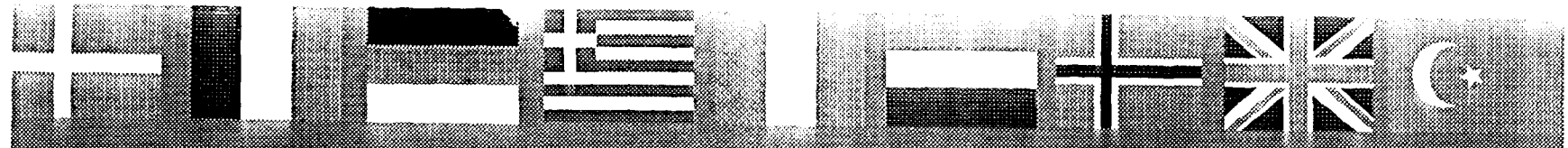


LPD "Rotterdam"
Fully Integrated Electric Propulsion



Future applications of PEBB in Europe

- Future European Escort Frigate / Corvette
- Future LPD's
- All Electric Vehicle
- etcetera



Capabilities

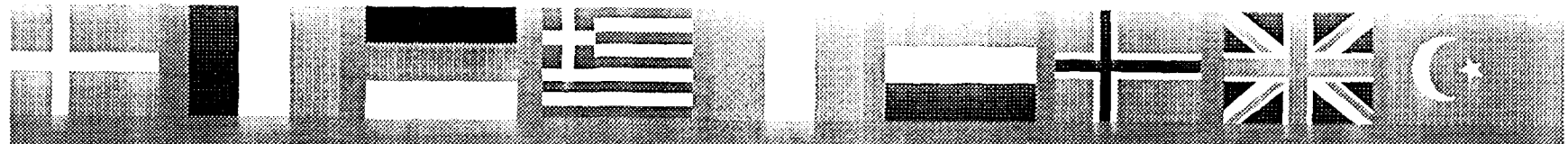
European companies with capabilities and performing R&D efforts are :

Global:

- a/o Cegelec, ABB, Siemens

as well as niche players:

- Holec



PEBB Conclusion

- There is no current PEBB initiative in Europe within the WEAG funded R&T projects
- Capable industries are present (Market Push)
- The application of PEBB is identified (Market Pull)
- In case PEBB is adopted by the CEPA, the initiative fits in CEPA EE Terms of Reference